

# DR2 17.3" Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2009-08-03

REV : -2

*DY : Nopop Component*

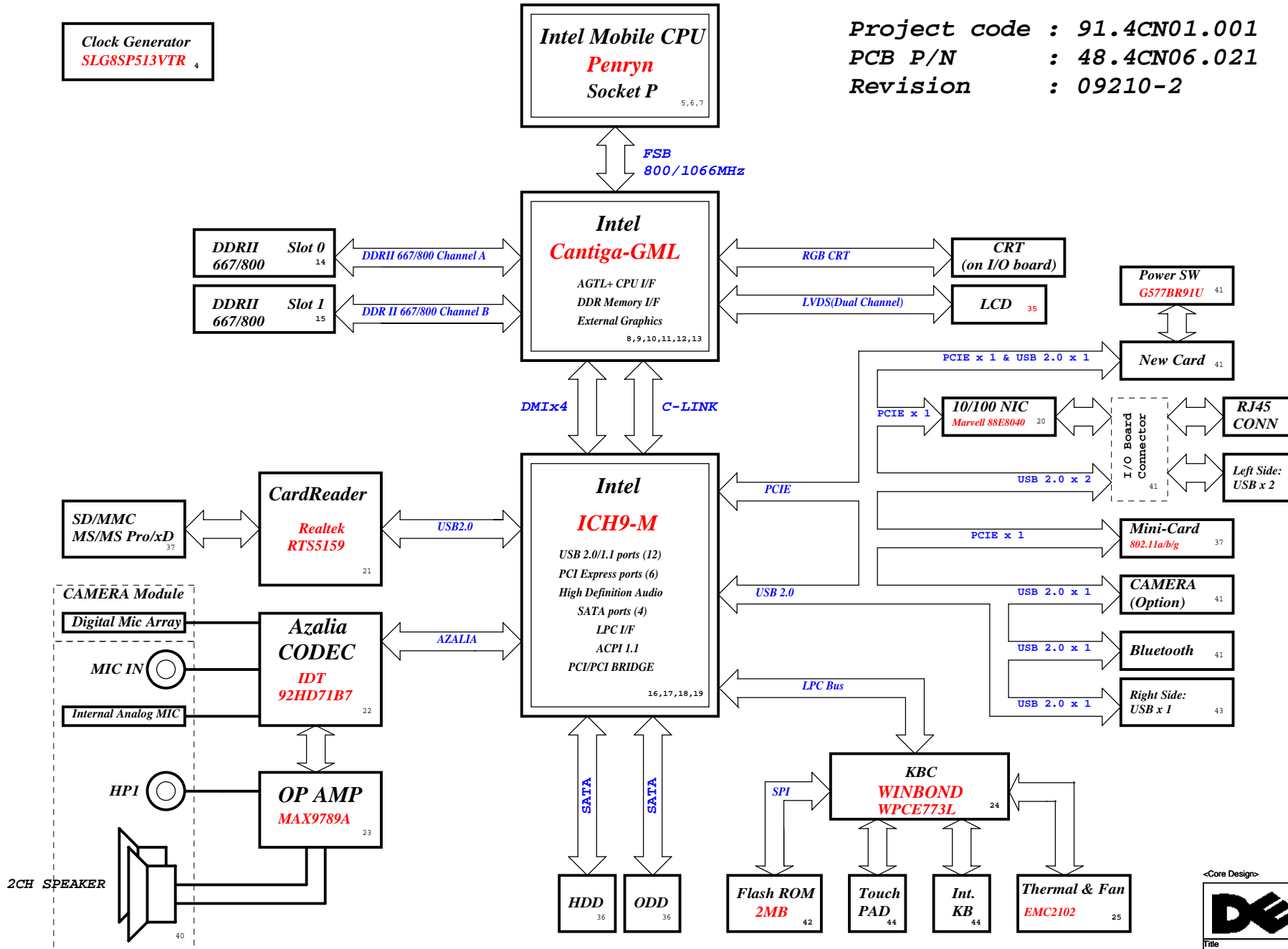
<Core Design>



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# Roberts Block Diagram



CPU DC/DC	
ISL6266A 28,29	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC	
TPS51117 30	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC	
MAX17020 27	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC	
TPS51116 31	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC	
APL5912 32	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC	
LDO 34	
INPUTS	OUTPUTS
+5V_ALW +3.3V_ALW	+5V_RUN +3.3V_RUN

MAXIM CHARGER	
MAX8731A 26	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

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Rev: 2

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1 Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

# ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS_LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: {3->0, 2->1, 1->2 and 0->3 DMI x2 mode [MCH->ICH]: {3->0, 2->1}
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

## NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

## PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

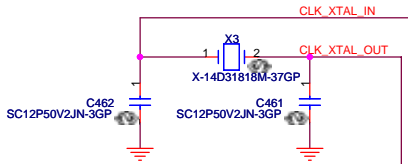
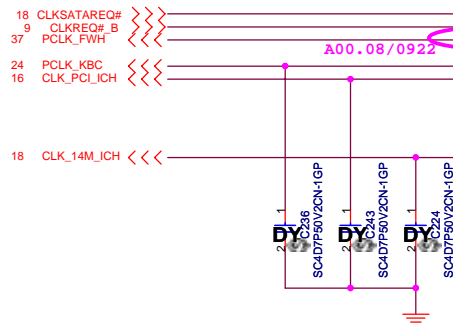
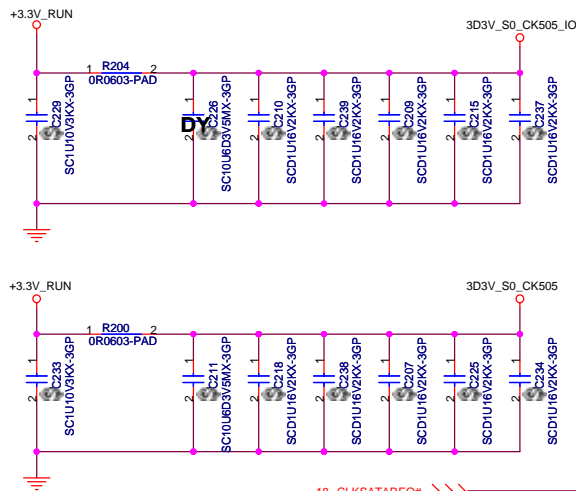
## USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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SSID = CLOCK

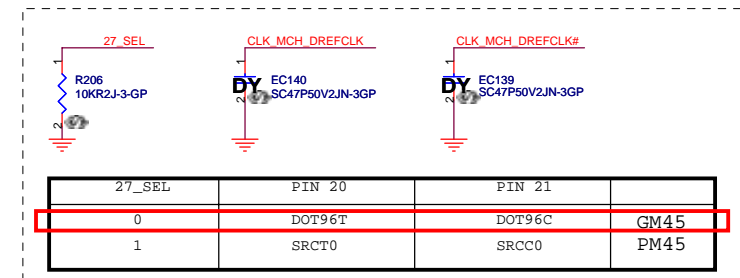
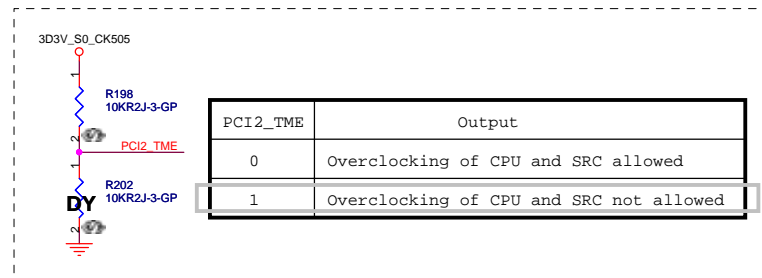
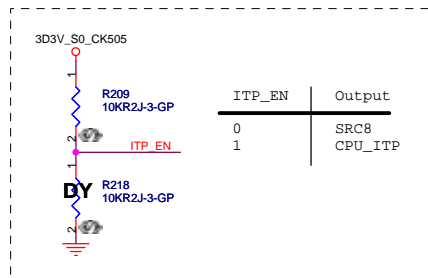


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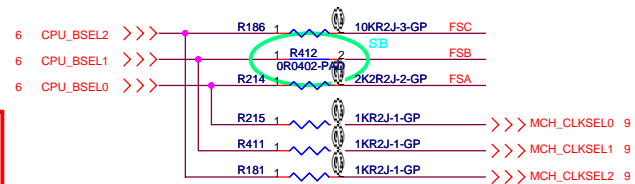


Main source: 71.08513.003 (SLG8SP513VTR)  
2nd source: 71.00875.C03 (RTM875N-606-VD-GR1)  
3rd source:

Co-layout Ref: 71.09355.B03 (ICS9LPRS355BKLFT)



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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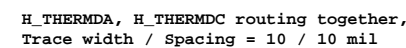
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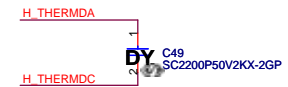
Size: Custom Document Number: **DR2 17" UMA** Rev: **2**

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5  
SSID = CPU



H\_THRMTRIP# should connect to ICH9 and MCH without T-ing.



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Title	Author	Year	Journal	Volume	Page
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**CPU-FSB(1/3)**

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Date: Monday, August 03, 2009

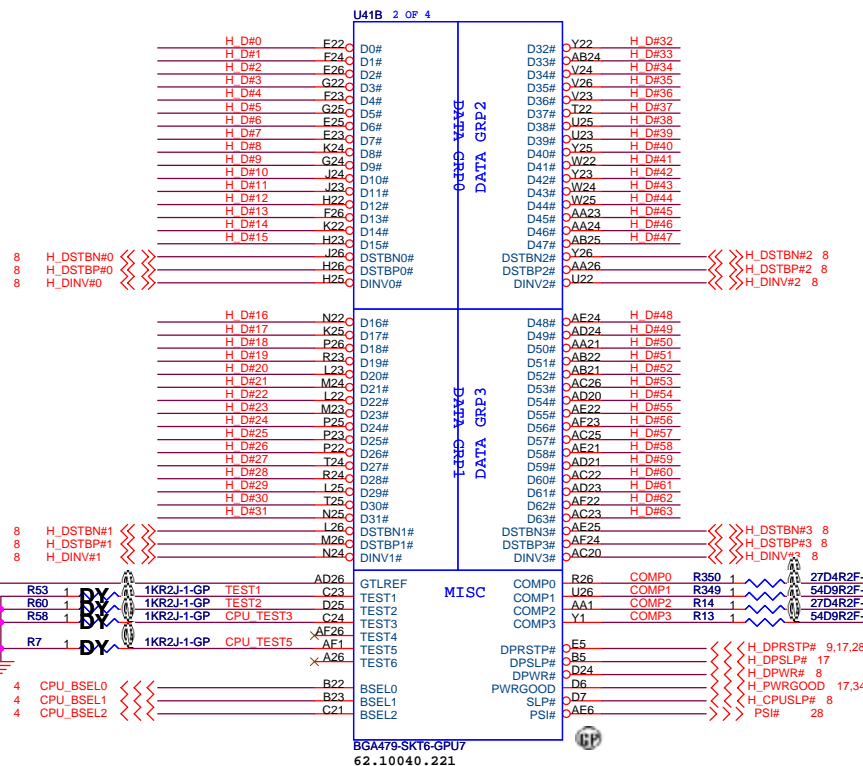
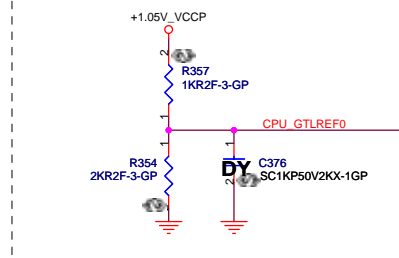
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SSID = CPU

H\_DINV#[3..0] << >> H\_DINV#[3..0] 8  
H\_DSTBN#[3..0] << >> H\_DSTBN#[3..0] 8  
H\_DSTBP#[3..0] << >> H\_DSTBP#[3..0] 8  
H\_D#[63..0] << >> H\_D#[63..0] 8

#### Layout notes

Z= 55 Ohm 0.5" MAX for CPU\_GTLREF0



Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Route the CPU\_TEST3 and CPU\_TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

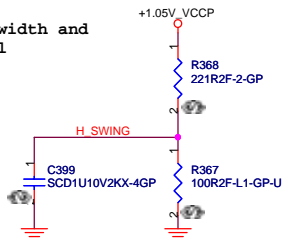
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SSID = MCH

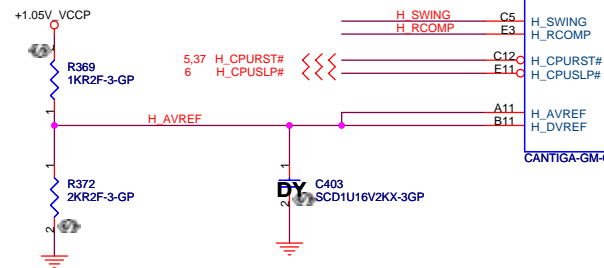
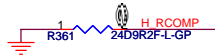
H\_SWING routing Trace width and  
Spacing use 10 / 20 mil

H\_SWING Resistors and  
Capacitors close MCH  
500 mil ( MAX )



H\_RCOMP routing Trace width and  
Spacing use 10 / 20 mil

Place R51 near to the chip ( < 0.5")



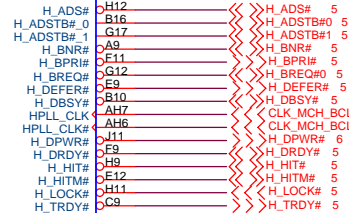
U52A

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H\_A#(35..3]

H\_A#(35..3]

HOST



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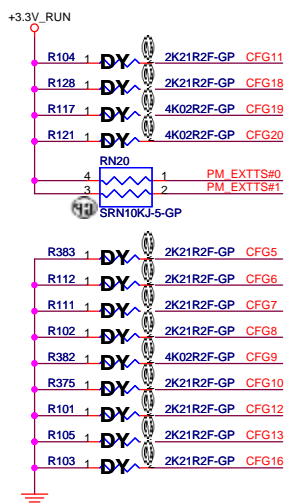




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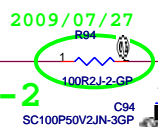
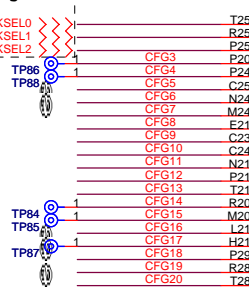
\* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in order *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19	Normal operation *	Reverse DMI lanes
DMI Lane Reserved		
CFG 20	Only PCIE or SDVO is operational *	PCIE and SDVO are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



18,24,25 PM\_PWROK >>>  
16,20,21,24,37,41 PLT\_RST# >>>  
5,17,24,34 H\_THRMTRIP# >>>  
18,28 DPRSLPVR >>>

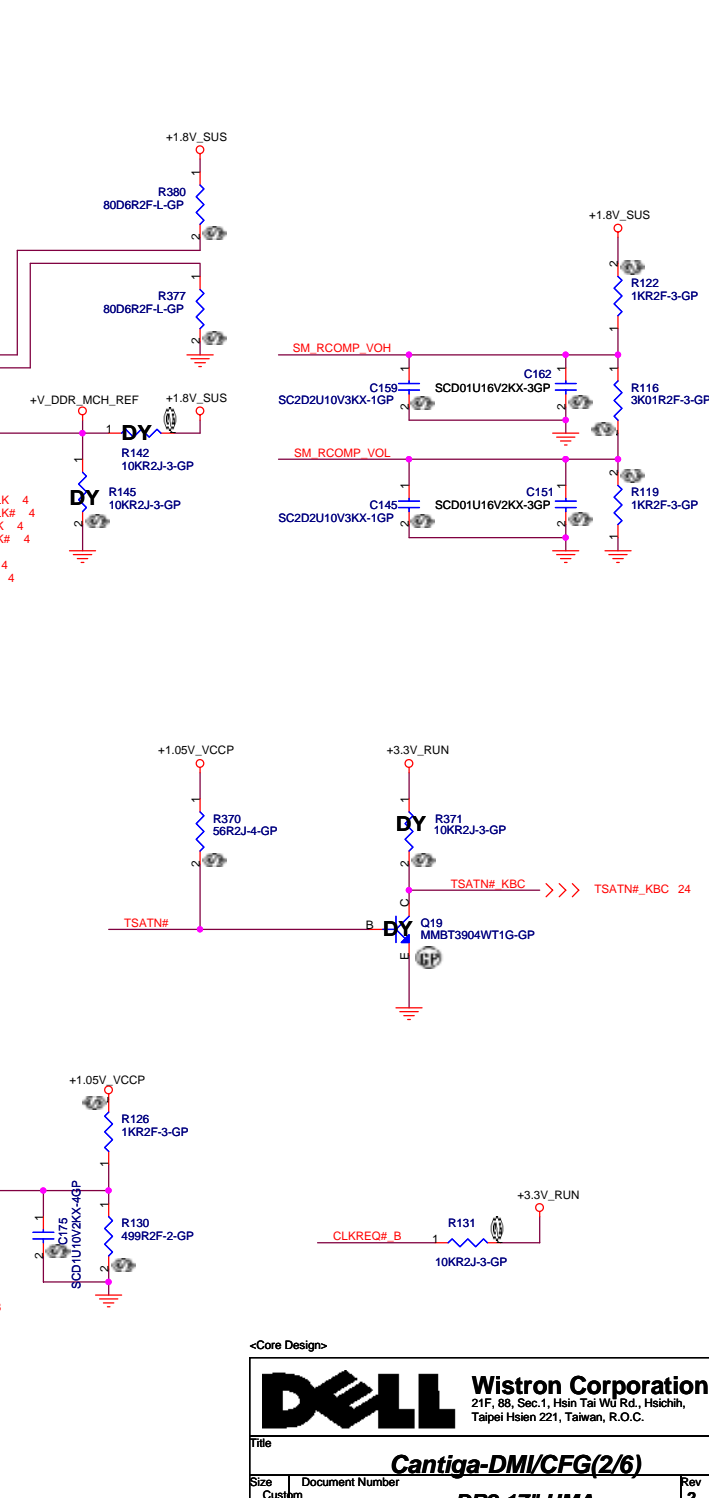
FSB setting



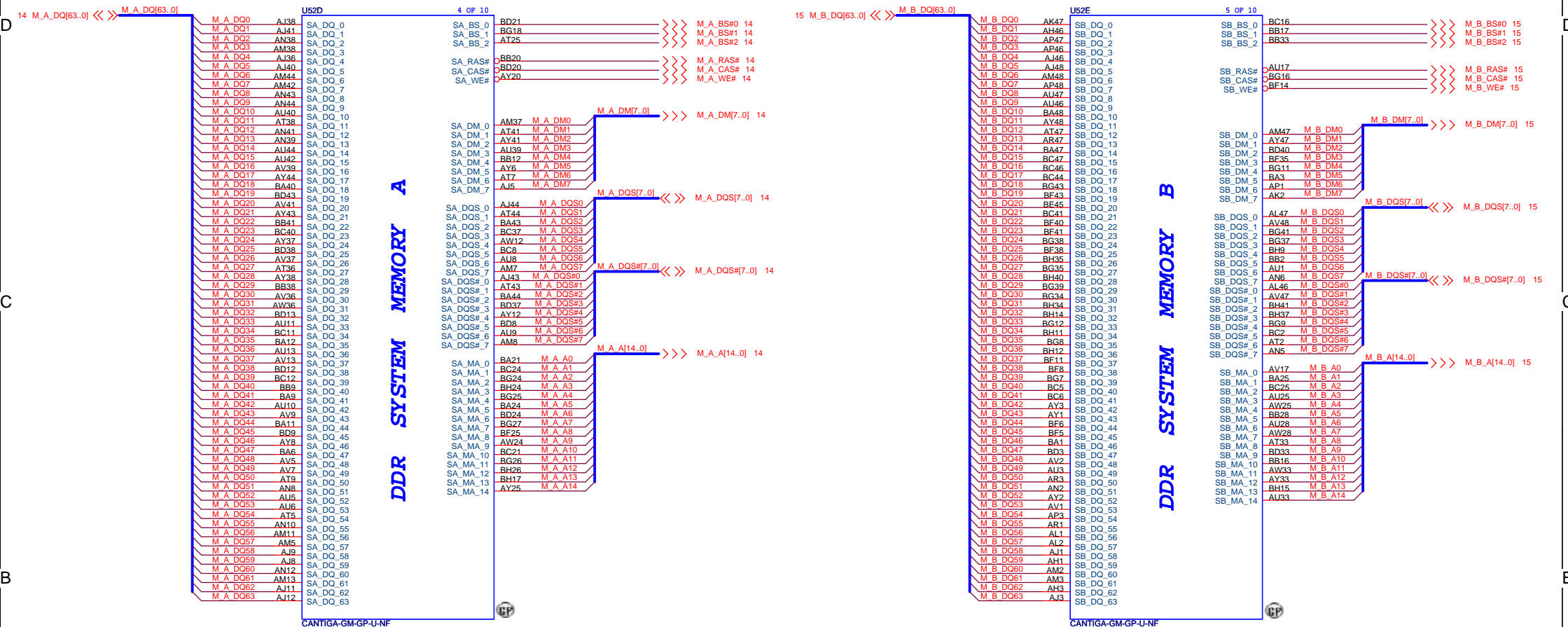
M36	RESERVED#M36	CFG.0	NC#BG48
N36	RESERVED#N36	CFG.1	NC#BF48
R33	RESERVED#R33	CFG.2	NC#BD48
T33	RESERVED#T33	CFG.3	NC#BC48
AH9	RESERVED#AH9	CFG.4	NC#BH47
AH10	RESERVED#AH10	CFG.5	NC#BG47
AH12	RESERVED#AH12	CFG.6	NC#BE47
AH13	RESERVED#AH13	CFG.7	NC#BH46
K12	RESERVED#K12	CFG.8	NC#BF46
AL34	RESERVED#AL34	CFG.9	NC#BG45
AK34	RESERVED#AK34	CFG.10	NC#BH44
AM35	RESERVED#AM35	CFG.11	NC#BD43
AN35	RESERVED#AN35	CFG.12	NC#BE43
T24	RESERVED#T24	CFG.13	NC#BH43
B31	RESERVED#B31	CFG.14	NC#BG42
B2	RESERVED#B2	CFG.15	NC#BE42
M1	RESERVED#M1	CFG.16	NC#BH42
AY21	RESERVED#AY21	CFG.17	NC#BG2
BG23	RESERVED#BG23	CFG.18	NC#BE2
BF23	RESERVED#BF23	CFG.19	NC#BH41
BH18	RESERVED#BH18	CFG.20	NC#BG1
BF18	RESERVED#BF18		NC#BE1

U52B	2 OF 10
RSVD	DDR CLK/ CONTROL/COMPENSATION
CFG	CFG
DMI	DMI
GRAPHICS VID	GRAPHICS VID
ME	ME
MISC	MISC
HDA	HDA

SA_CLK_0	AP24	M_CLK_DDR0	14
SA_CLK_1	AT21	M_CLK_DDR1	14
SB_CLK_0	AV24	M_CLK_DDR2	15
SB_CLK_1	AU20	M_CLK_DDR3	15
SA_CLK#_0	AR24	M_CLK_DDR#0	14
SA_CLK#_1	AR21	M_CLK_DDR#1	14
SB_CLK#_0	AU24	M_CLK_DDR#2	15
SB_CLK#_1	AV20	M_CLK_DDR#3	15
SA_CKE_0	BC28	M_CKE0	14
SA_CKE_1	AY28	M_CKE1	14
SB_CKE_0	AY36	M_CKE2	15
SB_CKE_1	BB36	M_CKE3	15
SA_CS#_0	BA17	M_CS#0	14
SA_CS#_1	AY16	M_CS#1	14
SB_CS#_0	AV16	M_CS#2	15
SB_CS#_1	AR13	M_CS#3	15
SA_ODT_0	BD17	M_ODT0	14
SA_ODT_1	AY17	M_ODT1	14
SB_ODT_0	BE15	M_ODT2	15
SB_ODT_1	AY13	M_ODT3	15
SM_RCOMP	BG22	M_RCOMP	
SM_RCOMP_VOH	BH21	M_RCOMP	
SM_VREF	BE28	M_RCOMP_VOH	
SM_PWROK	BH28	M_RCOMP_VOL	
SM_EXT#	BC36		
SM_DRAMRST#			
DPLL_REF_CLK	AV42		
DPLL_REF_CLK#	AR36		
DPLL_REF_SSCLK	BE17		
DPLL_REF_SSCLK#	BC36		
CLK_MCH_DREFCLK	B38		
CLK_MCH_DREFCLK#	A38		
MCH_SSCDREFCLK	E41		
MCH_SSCDREFCLK#	F41		
CLK_MCH_3GPLL	F43		
CLK_MCH_3GPLL#	E43		
DMI_RXN_0	AE41		
DMI_RXN_1	AE37		
DMI_RXN_2	AE47		
DMI_RXN_3	AH39		
DMI_TXP_0	AE40		
DMI_TXP_1	AE38		
DMI_TXP_2	AE48		
DMI_TXP_3	AH40		
DMI_RXN_0	AE35		
DMI_RXN_1	AE43		
DMI_RXN_2	AE46		
DMI_RXN_3	AH42		
DMI_RXP_0	AD35		
DMI_RXP_1	AE44		
DMI_RXP_2	AE46		
DMI_RXP_3	AH43		
GFX_VID_0	B33		
GFX_VID_1	B32		
GFX_VID_2	G33		
GFX_VID_3	F33		
GFX_VID_4	E33		
GFX_VR_EN	C34		
CL_CLK	AH37		
CL_DATA	AH36		
CL_PWROK	AN36		
CL_RST#	AY35		
CL_VREF	AH34		
DDPC_CTRLCLK	N28		
DDPC_CTRLDATA	M28		
SDVO_CTRLCLK	G36		
SDVO_CTRLDATA	E36		
CLKREQ#	K36		
ICH_SYNC#	H36		
TSATN#	B12		
HDA_BCLK	B28		
HDA_RST#	B30		
HDA_SD	B29		
HDA_SDO	C29		
HDA_SYNC	A28		



SSID = MCH



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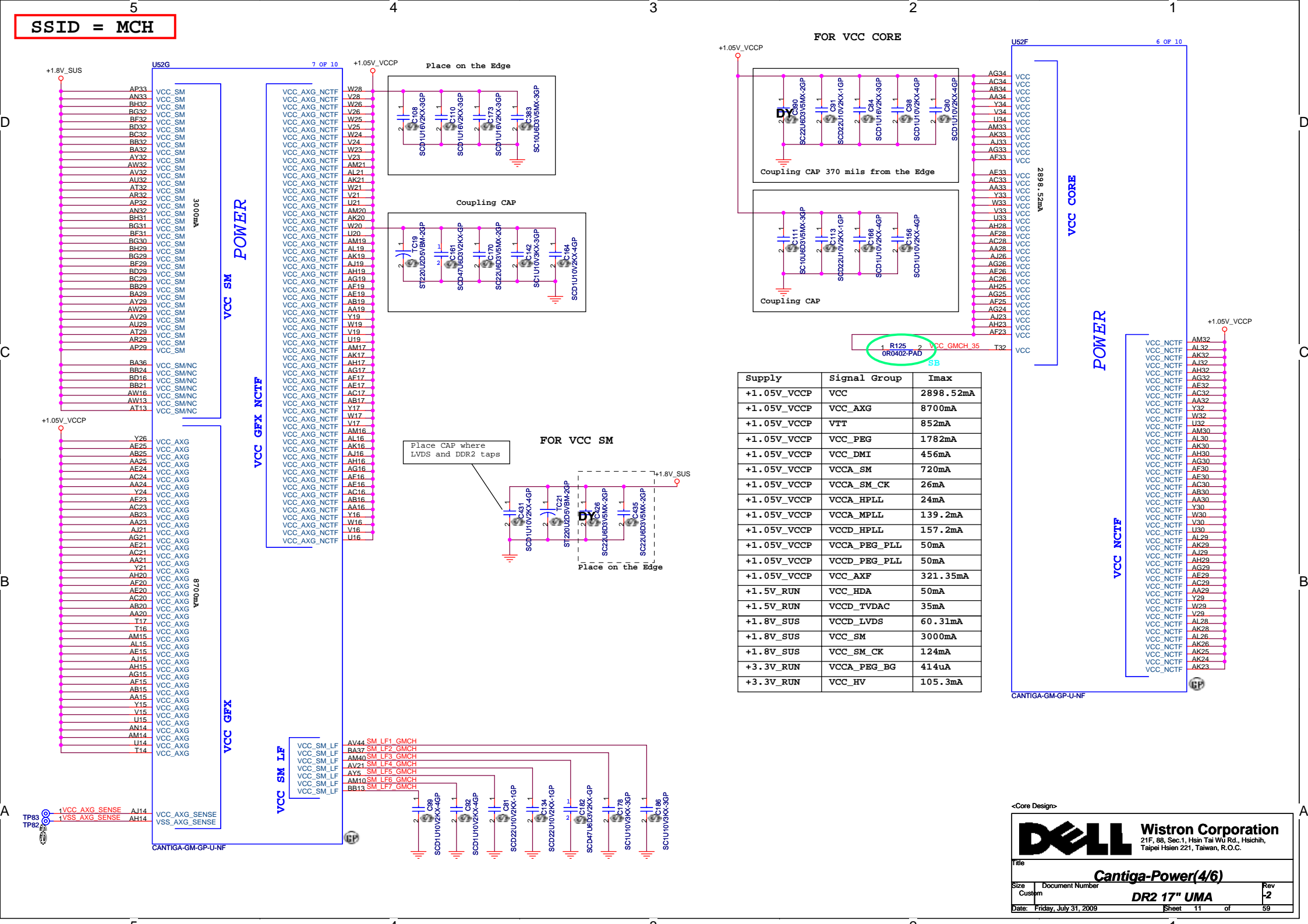
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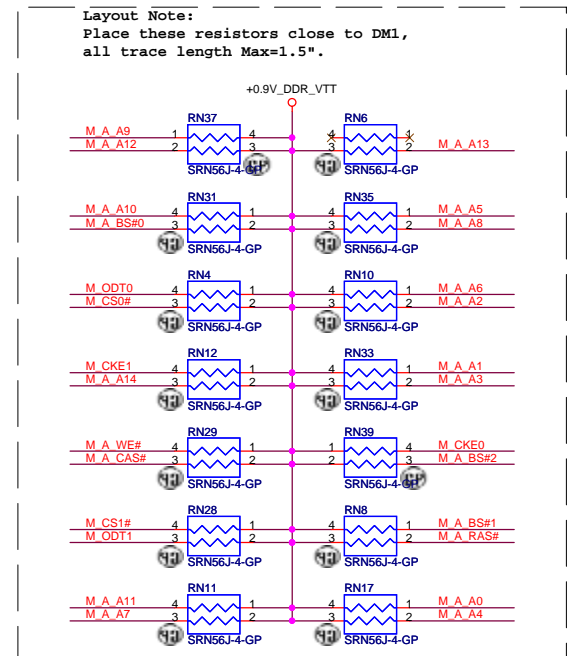
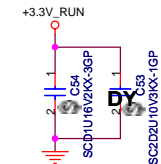
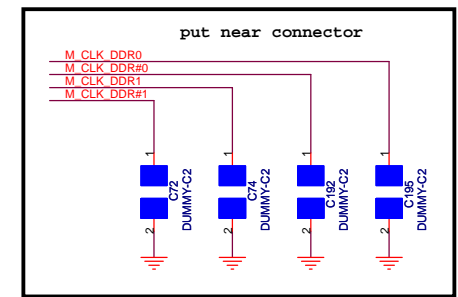
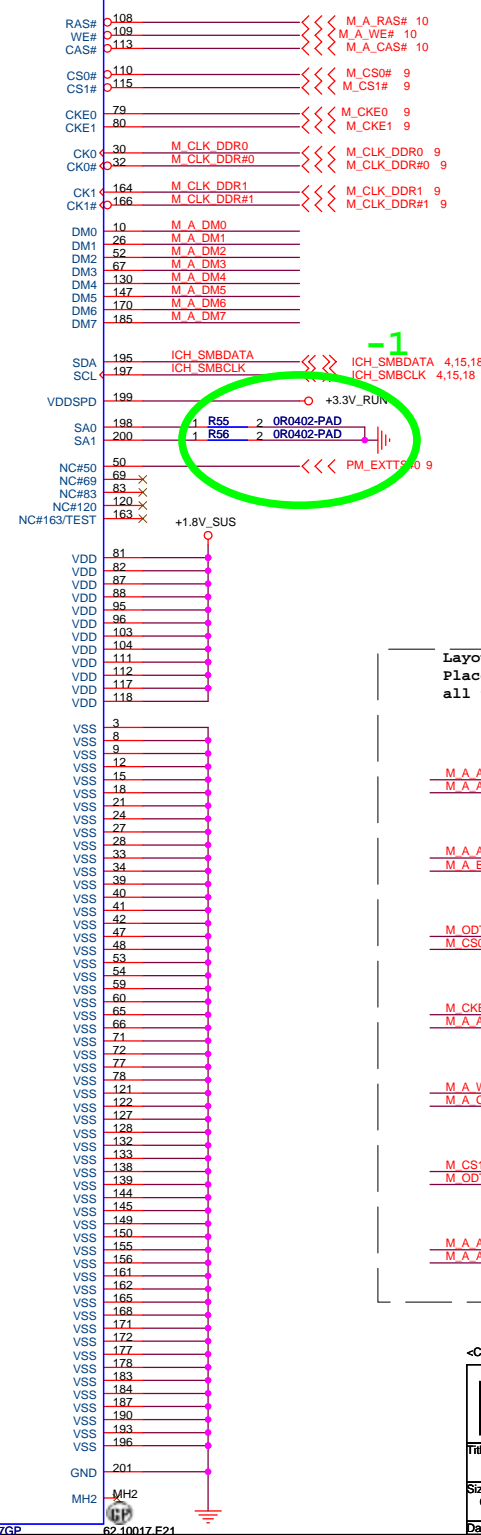
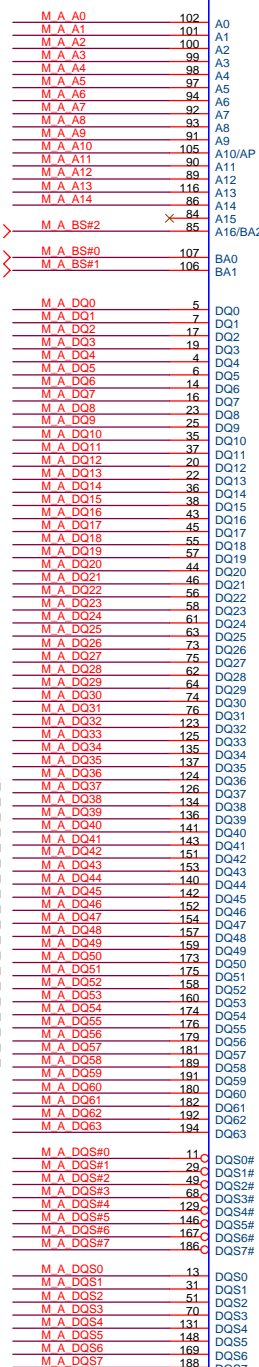
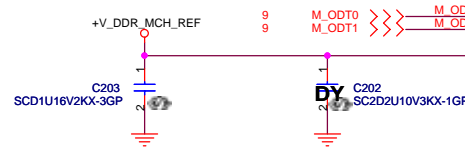
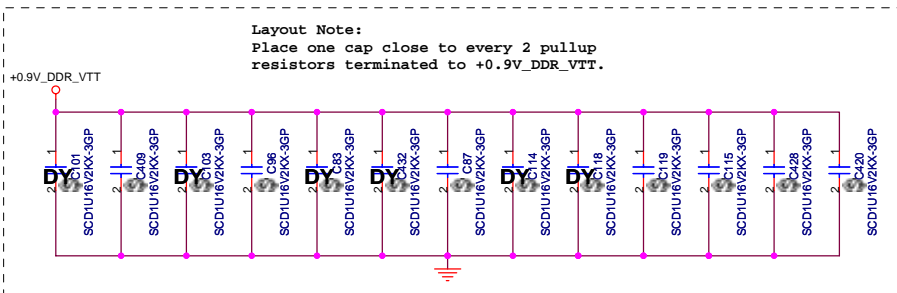
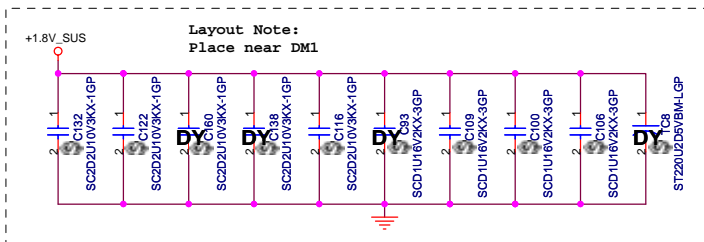
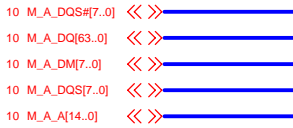


SSID = MCH



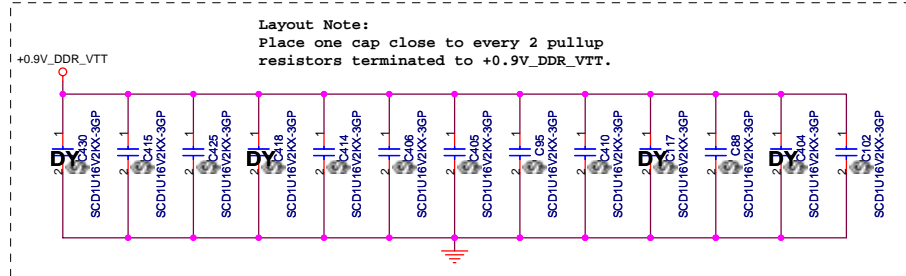
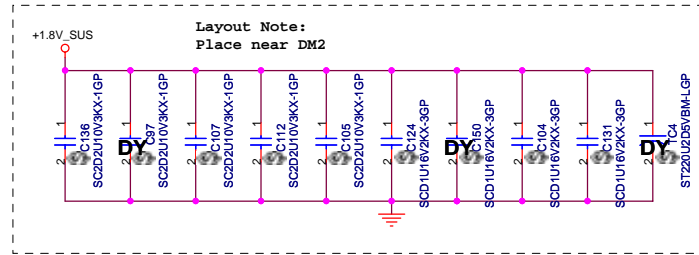


**SSID = MEMORY**



SSID = MEMORY

10 M\_B\_DQS#7..0 <<>>  
10 M\_B\_DQ[63..0] <<>>  
10 M\_B\_DM[7..0] <<>>  
10 M\_B\_DQS[7..0] <<>>  
10 M\_B\_A[14..0] <<>>

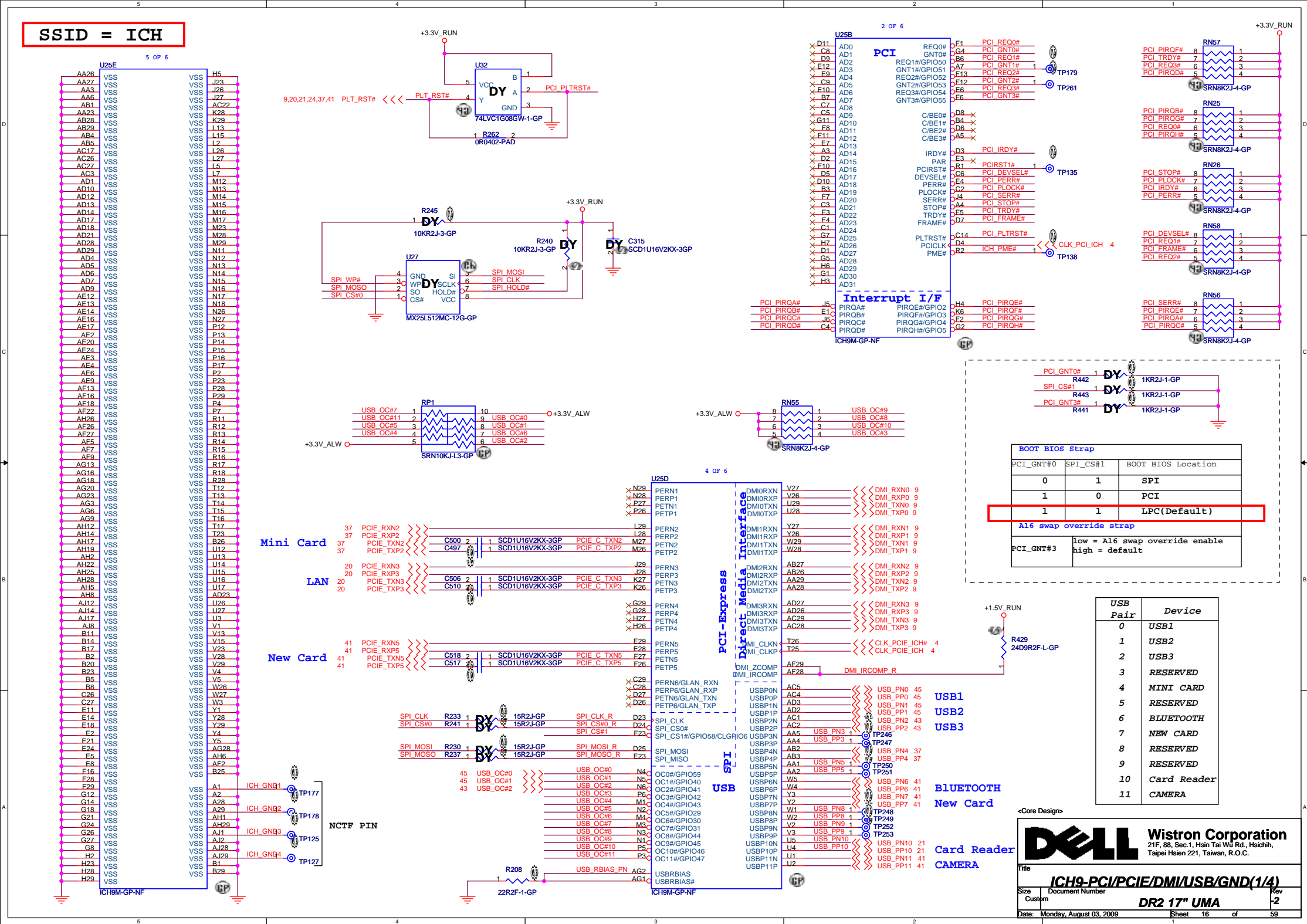


10 M\_B\_BS#2 >>> M\_B\_BS#2

10 M\_B\_BS#0 >>> M\_B\_BS#0  
10 M\_B\_BS#1 >>> M\_B\_BS#1

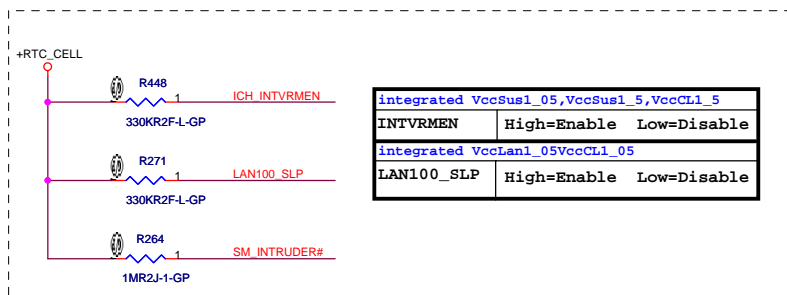
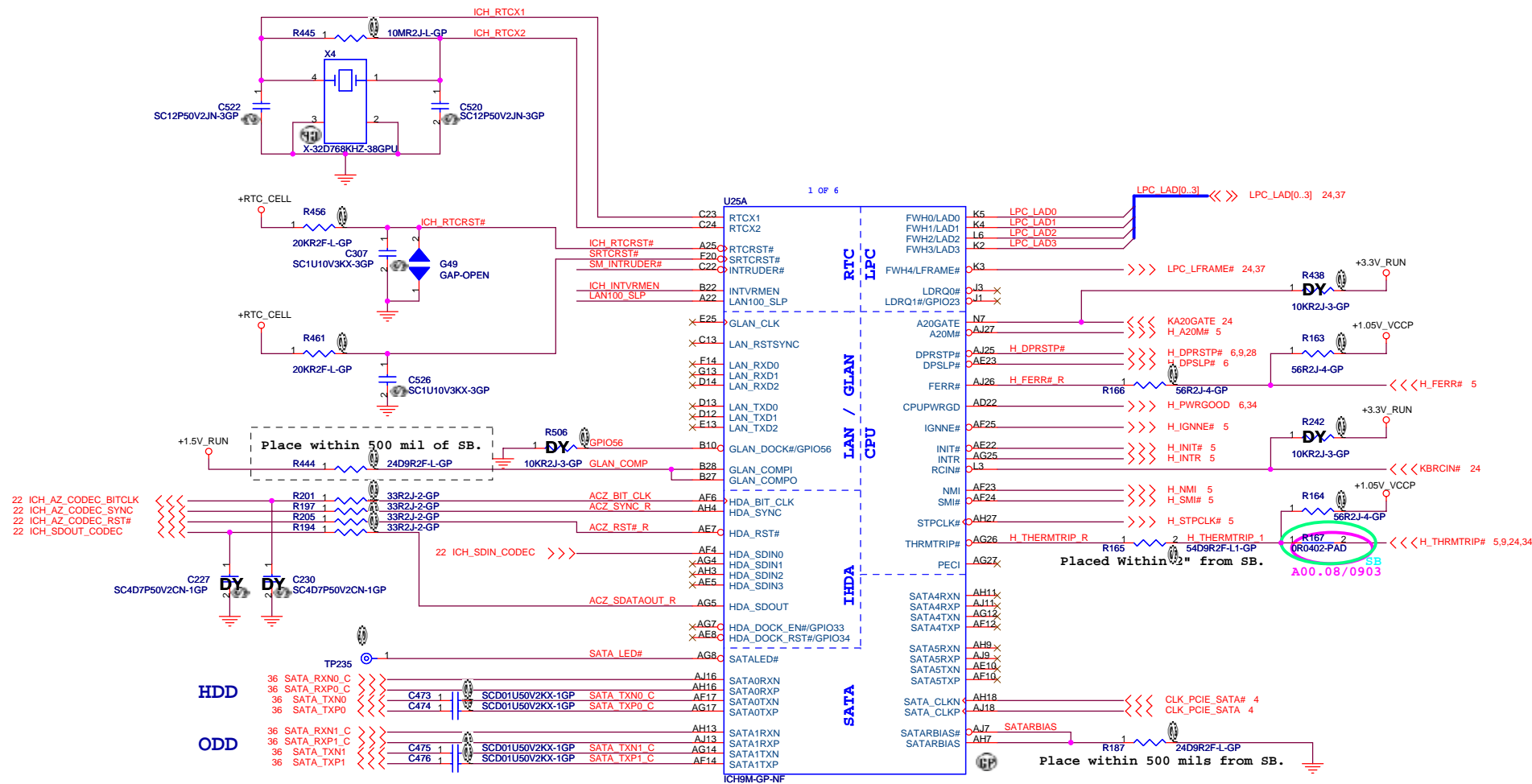
M_B_D00	5	D00
M_B_D01	7	D01
M_B_D02	17	D02
M_B_D03	19	D03
M_B_D04	4	D04
M_B_D05	6	D05
M_B_D06	14	D06
M_B_D07	16	D07
M_B_D08	23	D08
M_B_D09	25	D09
M_B_D010	35	D010
M_B_D011	37	D011
M_B_D012	20	D012
M_B_D013	22	D013
M_B_D014	36	D014
M_B_D015	38	D015
M_B_D016	43	D016
M_B_D017	45	D017
M_B_D018	57	D018
M_B_D019	57	D019
M_B_D020	44	D020
M_B_D021	46	D021
M_B_D022	56	D022
M_B_D023	58	D023
M_B_D024	61	D024
M_B_D025	63	D025
M_B_D026	73	D026
M_B_D027	75	D027
M_B_D028	77	D028
M_B_D029	64	D029
M_B_D030	74	D030
M_B_D031	76	D031
M_B_D032	123	D032
M_B_D033	125	D033
M_B_D034	132	D034
M_B_D035	135	D035
M_B_D036	124	D036
M_B_D037	126	D037
M_B_D038	134	D038
M_B_D039	136	D039
M_B_D040	141	D040
M_B_D041	143	D041
M_B_D042	151	D042
M_B_D043	153	D043
M_B_D044	140	D044
M_B_D045	142	D045
M_B_D046	152	D046
M_B_D047	154	D047
M_B_D048	157	D048
M_B_D049	159	D049
M_B_D050	173	D050
M_B_D051	175	D051
M_B_D052	158	D052
M_B_D053	160	D053
M_B_D054	174	D054
M_B_D055	176	D055
M_B_D056	181	D056
M_B_D057	181	D057
M_B_D058	189	D058
M_B_D059	181	D059
M_B_D060	192	D060
M_B_D061	192	D061
M_B_D062	192	D062
M_B_D063	194	D063

SSID = ICH





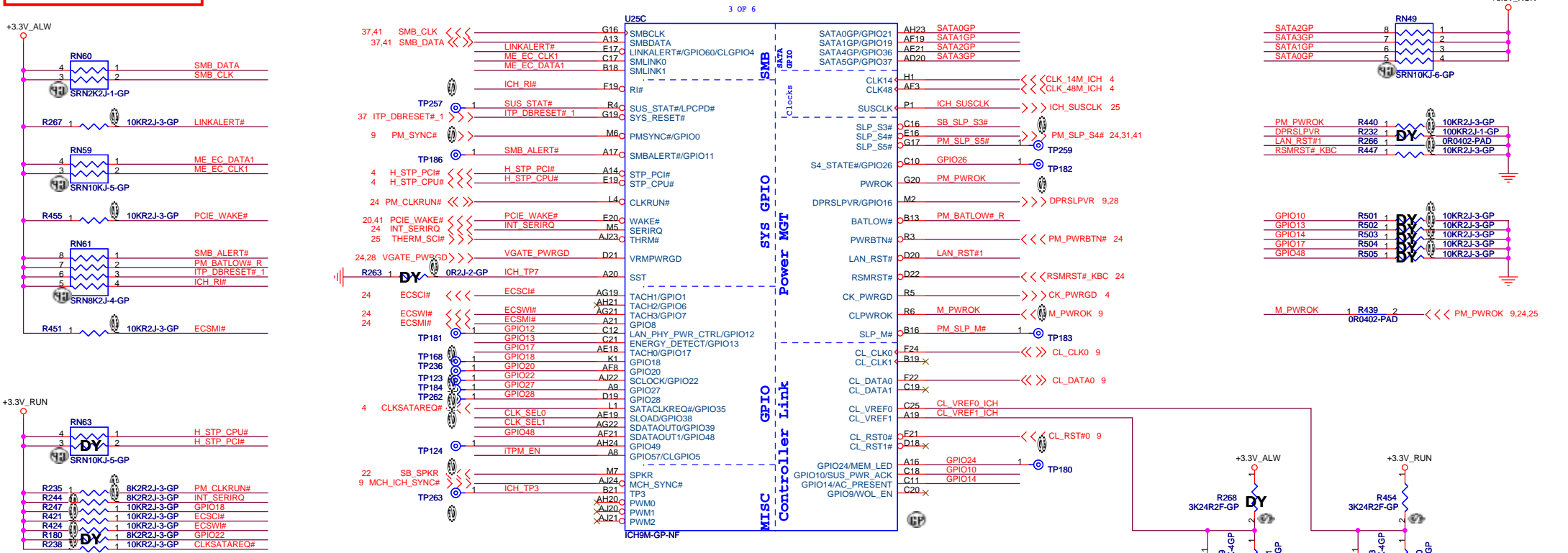
SSID = ICH



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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>ICH9-LAN/HDA/SATA/LPC(2/4)</b>			
Size	Document Number		Rev
Custom	<b>DR2 17" UMA</b>		<b>-2</b>
Date:	Monday, August 03, 2009	Sheet	17 of 59

SSID = ICH



ITPM Select

ITPM_EN
0 = Disable
1 = Enable

CLK Gen Select

CLK Gen	CLK_SELO	CLK_SEL1
Disable	X	X
Seligo	1	1
Realtek	1	0
ICS	0	1

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

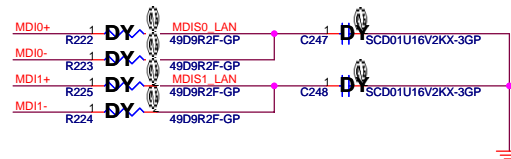
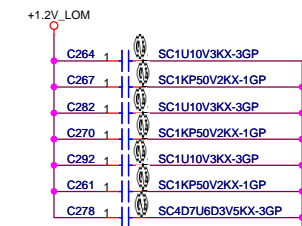
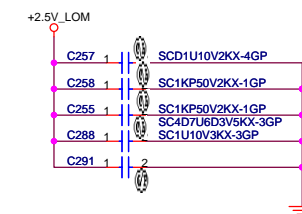
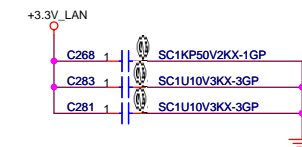
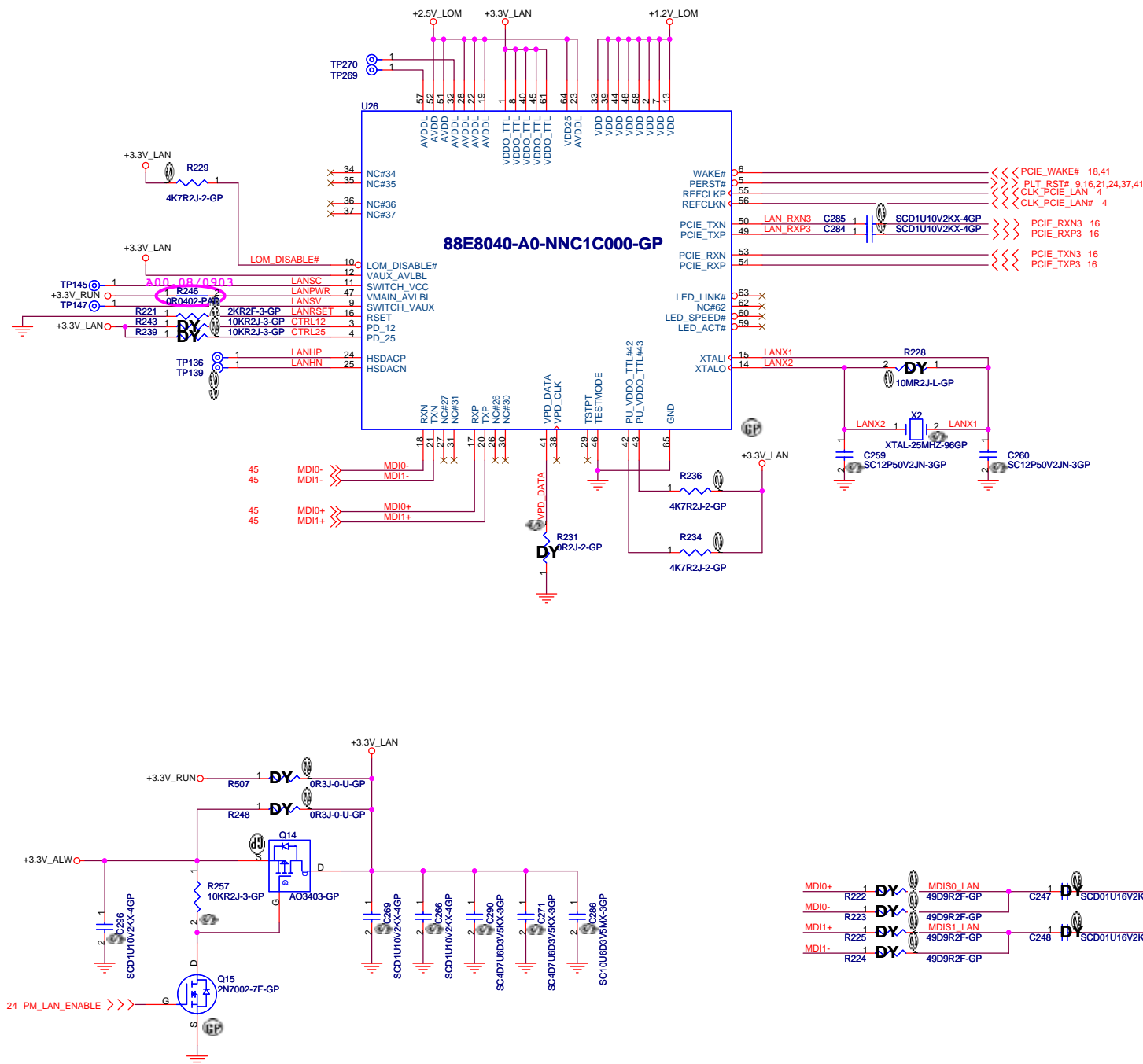
Title: **ICH9-GPIO/PM/CL(3/4)**

Size: Custom Document Number: **DR2 17" UMA** Rev: **2**

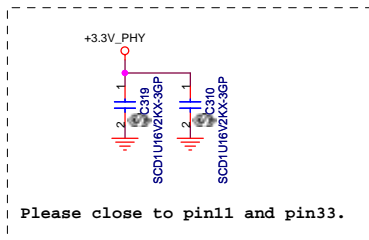
Date: Monday, August 03, 2009 Sheet 18 of 59



SSID = LOM



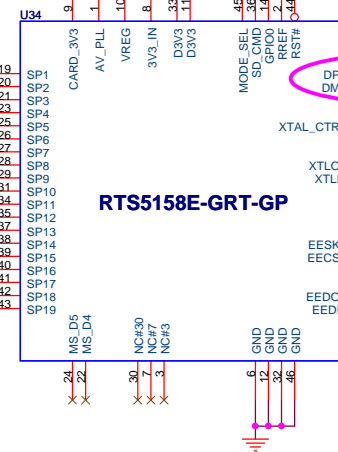
SSID = SDIO



Please close to pin8.

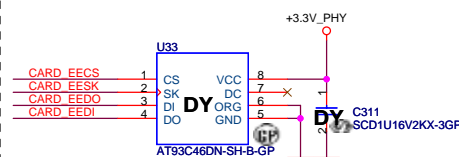
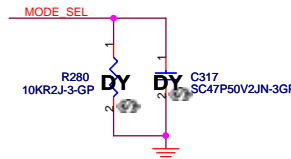
37 XD\_CD#  
37 SD\_WP  
37 SD\_CD#  
37 XD\_D4/SD\_DAT1  
37 XD\_D5/MS\_BS  
37 XD\_D3/MS\_D1  
37 SD\_DAT0/XD\_D6/MS\_D0  
37 XD\_D2/MS\_D2  
37 MS\_IN#  
37 XD\_D7/MS\_D3  
37 SD\_CLK/XD\_D1/MS\_CLK  
37 XD\_D0  
37 XD\_WP#  
37 XD\_RDY#  
37 SD\_DAT3/XD\_WE#  
37 SD\_DAT2/XD\_RE#  
37 XD\_ALE  
37 XD\_CE#  
37 XD\_CLE

SD\_WP  
SD\_CD#  
XD\_D4/SD\_DAT1  
XD\_D5/MS\_BS  
XD\_D3/MS\_D1  
SD\_DAT0/XD\_D6/MS\_D0  
XD\_D2/MS\_D2  
MS\_IN#  
XD\_D7/MS\_D3  
SD\_CLK/XD\_D1/MS\_CLK  
XD\_D0  
XD\_WP#  
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SD\_DAT2/XD\_RE#  
XD\_ALE  
XD\_CE#  
XD\_CLE

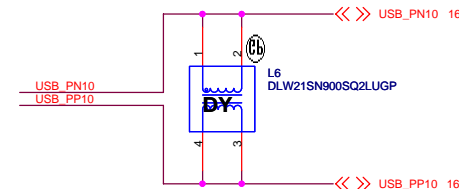


Power mode select

No staff R and C for power saving mode.



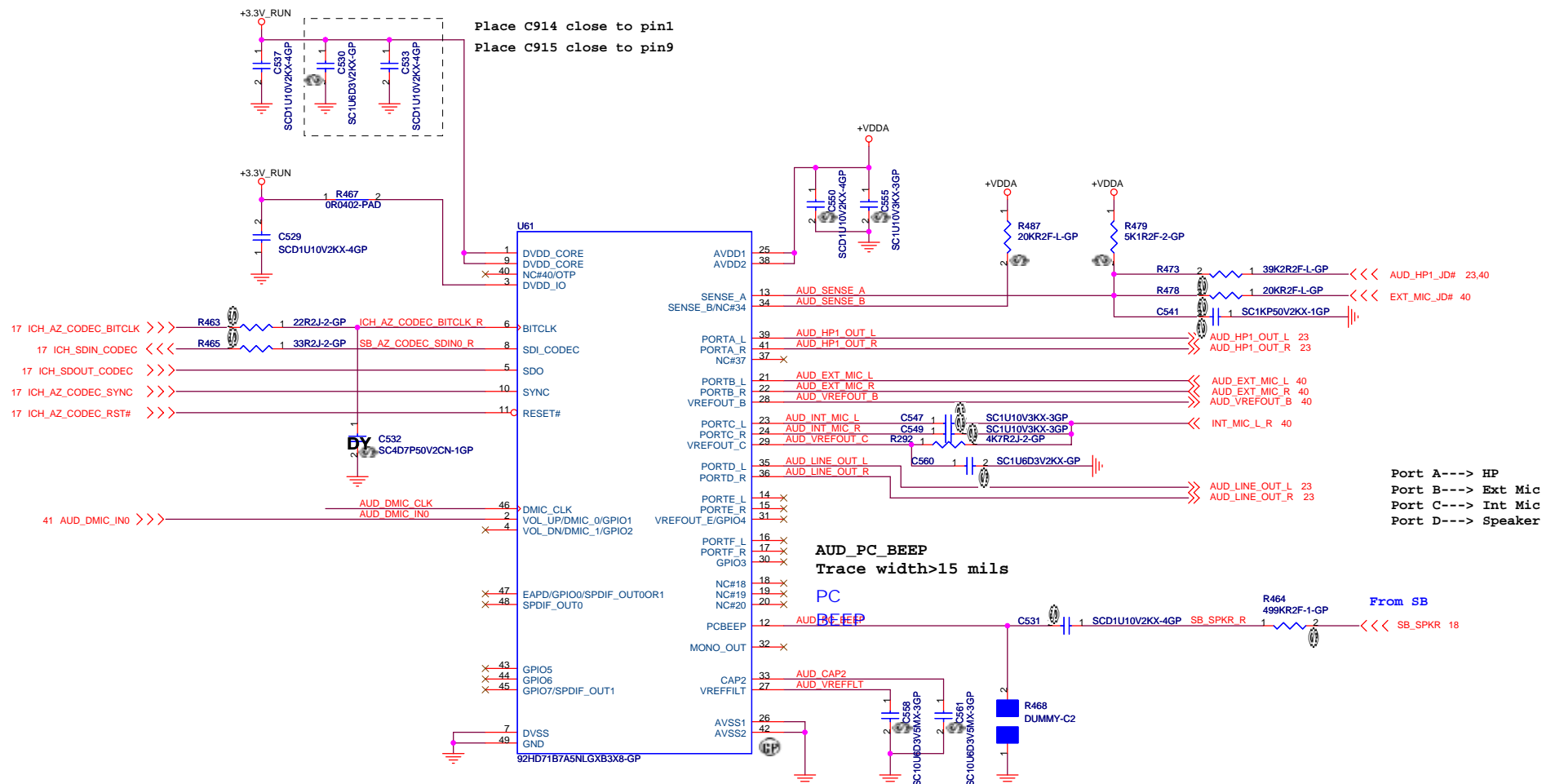
Reserve for changing USB VID/PID.



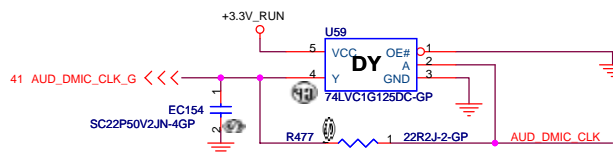
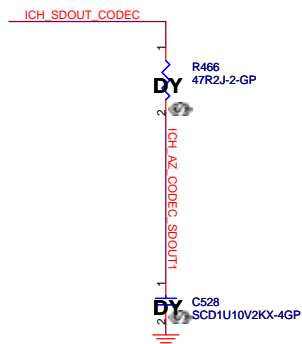
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RTS5158E			
Size	Document Number	Rev	
Custom	DR2 17" UMA	-2	
Date:	Monday, August 03, 2009	Sheet	21 of 59

## SSID = AUDIO



Azalia I/F EMI



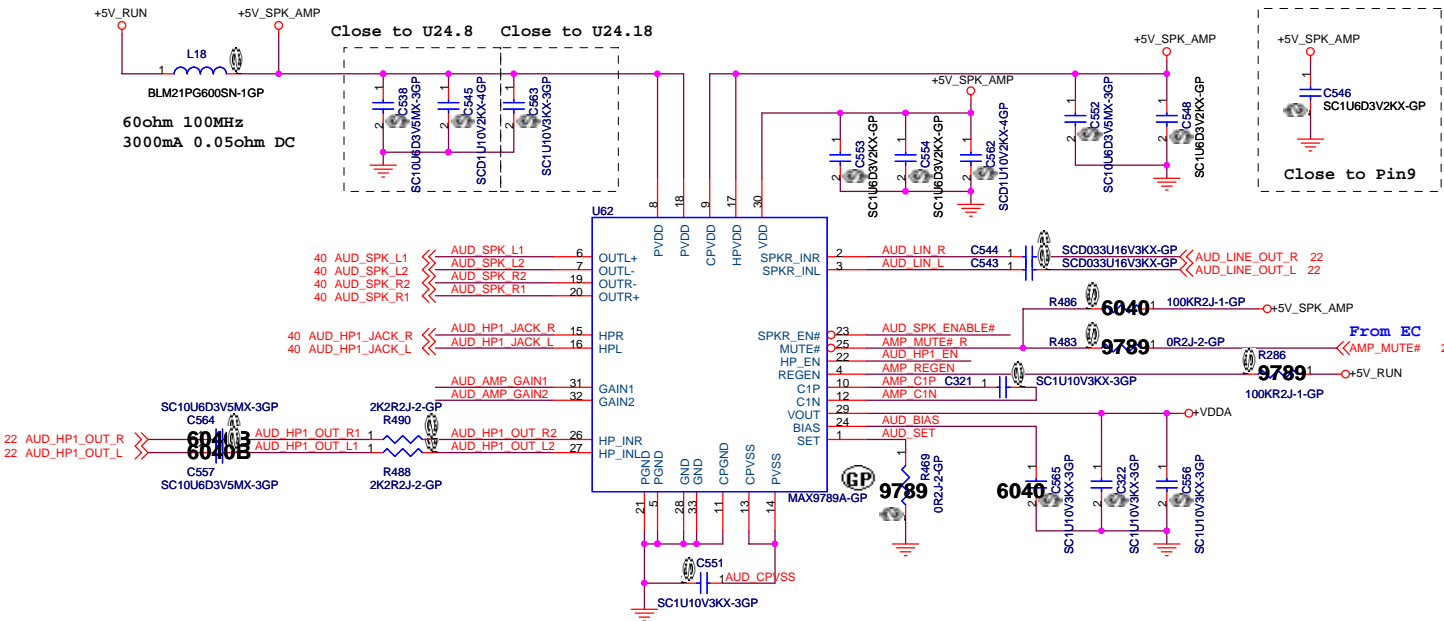
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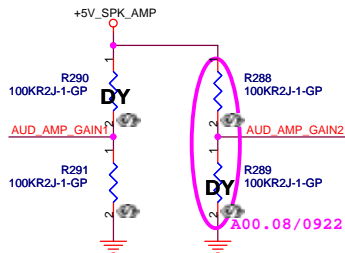
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>AUDIO CODEC 92HD71B7</b>			
Size	Document Number		Rev
Custom	<b>DR2 17" UMA</b>		<b>-2</b>
Date:	Monday, August 03, 2009	Sheet	22 of 59

# SSID = AUDIO

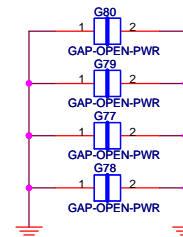


## GAIN SETTING

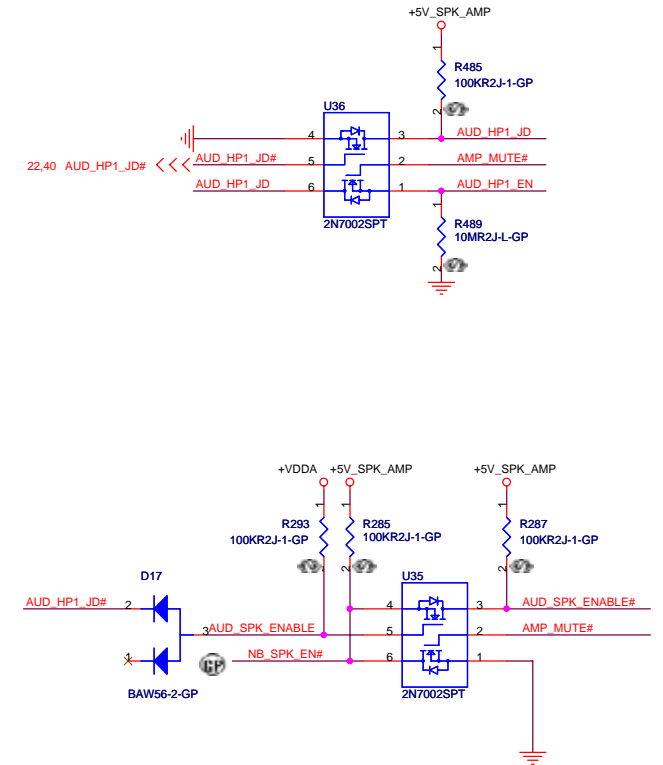


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF



## Signal inverter for speaker shutdown



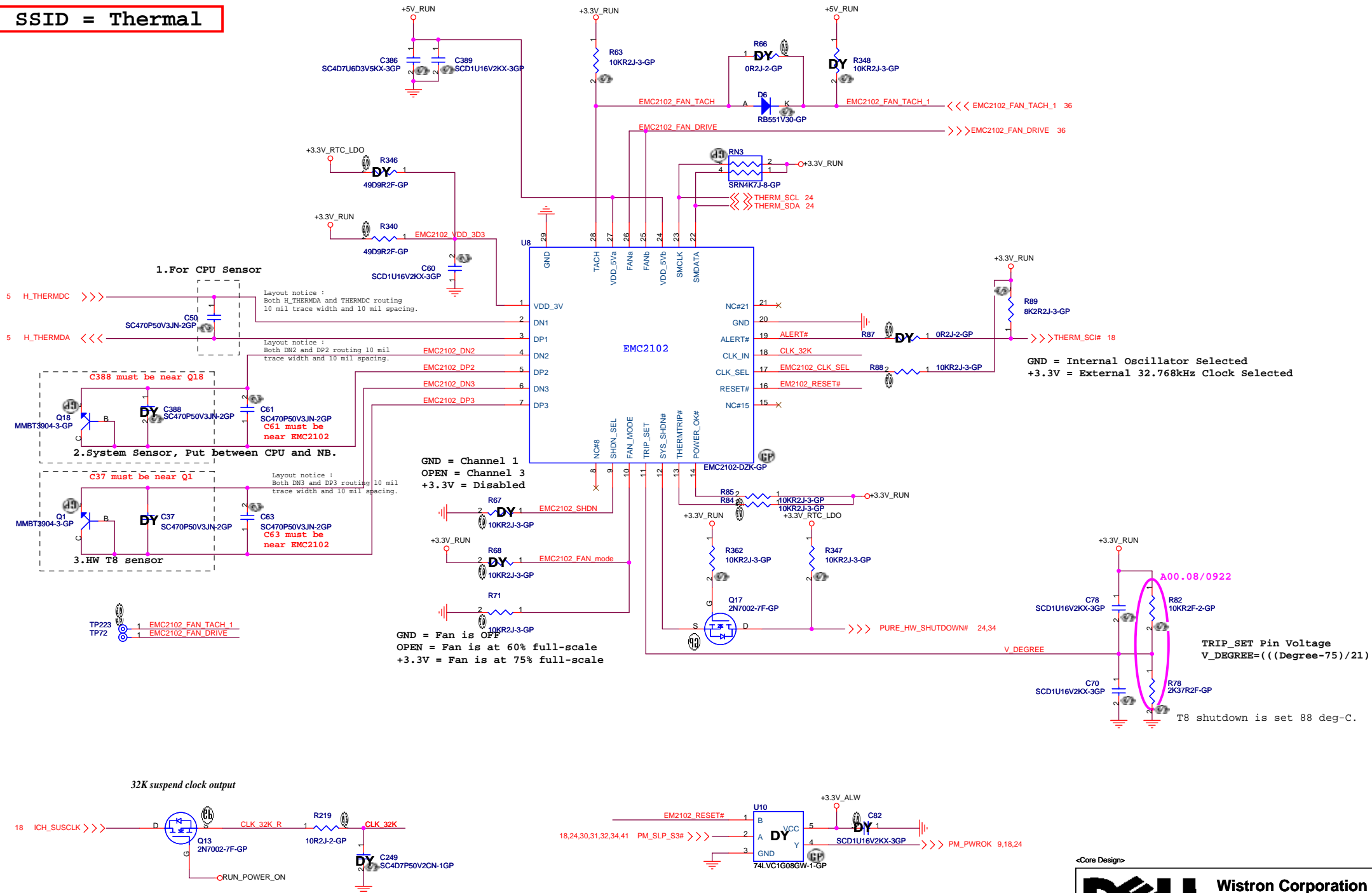
<Core Design>







# SSID = Thermal



<Core Design>



```
SSID = PWR.Plane.Regulator_3p3v5v
```

```

/P cap: 10U 25V K1206 X5R/ 78.10622.52L
uctor: 3.3UH PCMC06373R38NM CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
/P cap: 220U 6.3V PSLV0J2272M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
/P cap: 150U 6.3V PSLB20J157M(45) 45mohm 1.374Arms NEC_TOKIN/77.C1571.09L
/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

```

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation

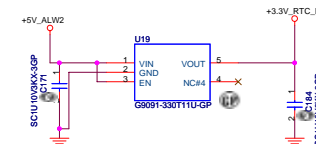
TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04

FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.30/3.345	1.038/1.050 /1.062	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 3.3UH P0MC06373R33JN CYNTEC DCR 28-30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: 220U 6.3V PSLV0J2272M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 150U 6.3V PSLB20J157M(45) 45mohm 1.374rms NEC\_TOKIN/77.C1571.09L  
H/S: IFR8707 SO-8/ 14.2mohm/ 17.5mOhm@4.5Vgs/ 84.08707.037  
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

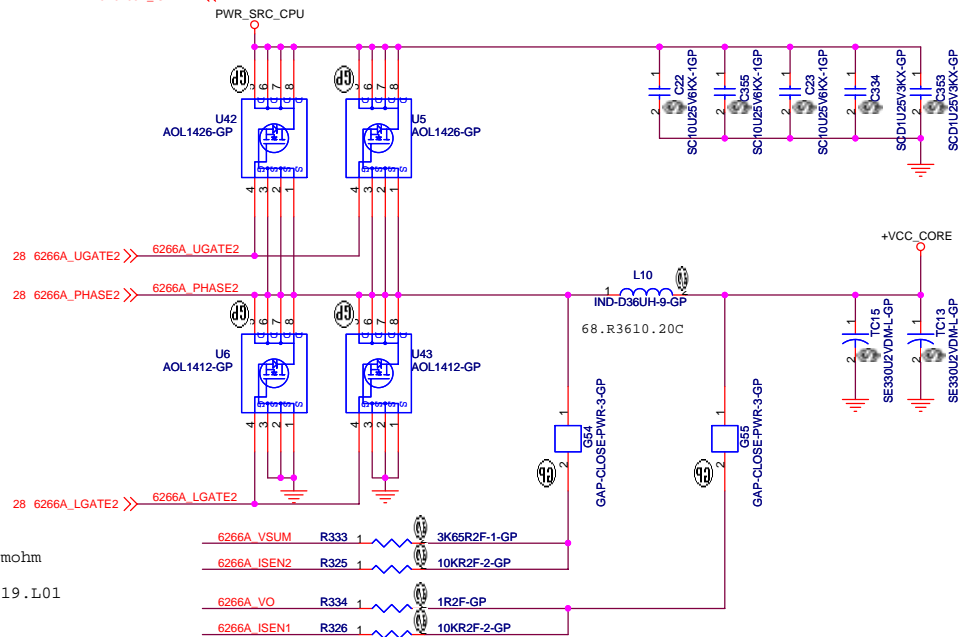
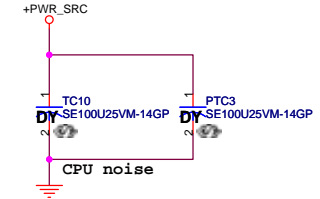
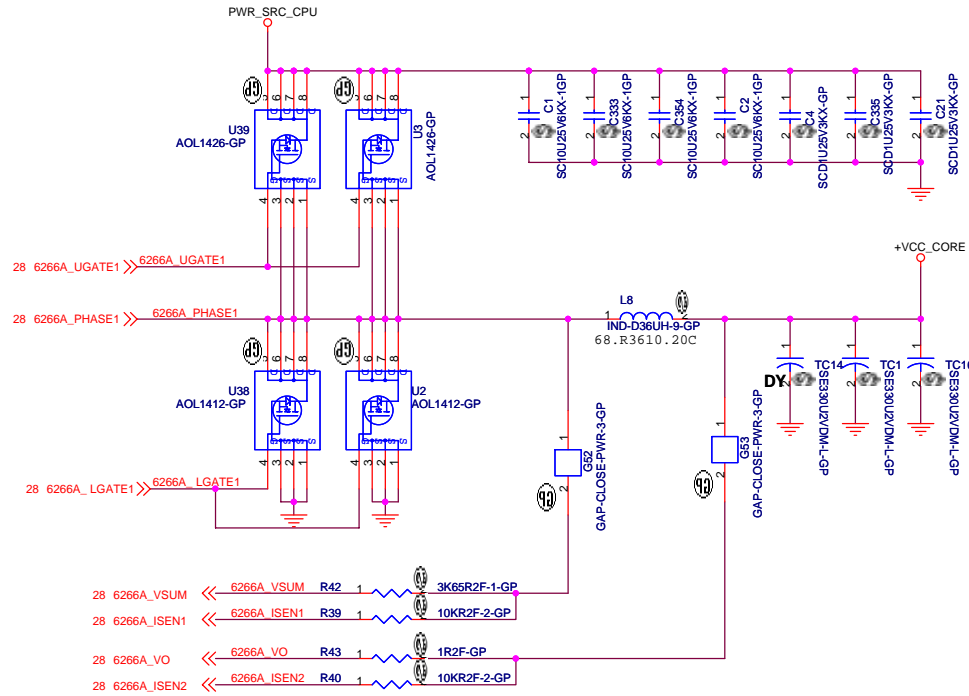
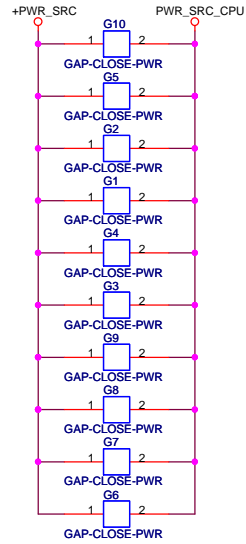


«Core Design»





**SSID = CPU.Regulator**

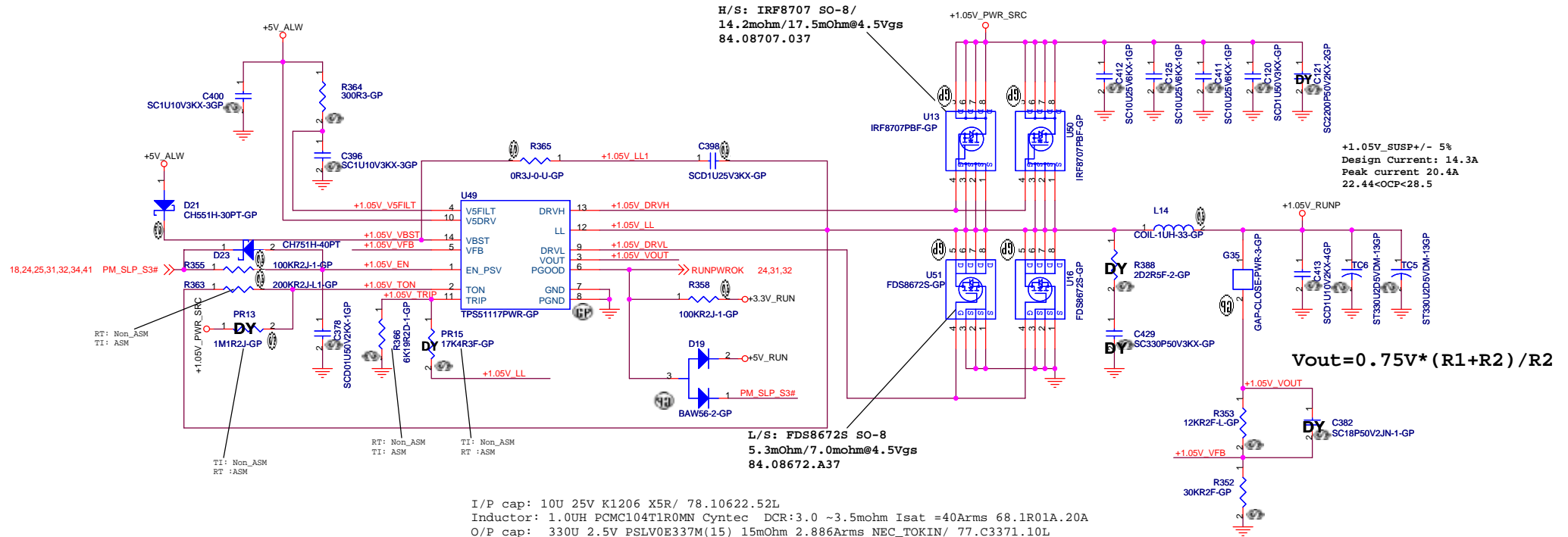
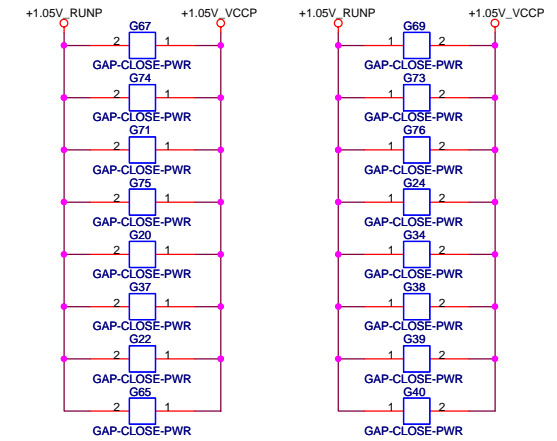
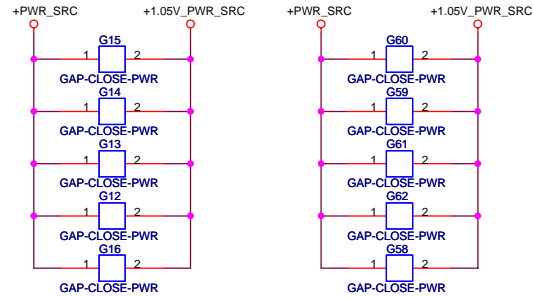


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm  
 Isat =60Arms 68.R3610.20C  
 O/P cap: 330U 2V EEF5X0D331ER 9mohm 3.0Arms Panasonic/79.33719.L01  
 H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mohm@4.5Vgs/84.01426.037  
 L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mohm@4.5Vgs/ 84.01412.037

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>CPU VCORE POWER(2/2)</b>	
Size	Document Number	Rev	
Custom		<b>DR2 17" UMA</b>	<b>-2</b>
Date:	Monday, August 03, 2009	Sheet	29 of 59

# SSID = PWR.Plane.Regulator\_1p05v



H/S: IRF8707 SO-8/  
14.2mohm/17.5mOhm@4.5Vgs  
84.08707.037

L/S: FDS8672S SO-8  
5.3mOhm/7.0mohm@4.5Vgs  
84.08672.A37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.0UH PCMC104T1R0MN Cyntec DCR:3.0 ~3.5mohm Isat =40Arms 68.1R01A.20A  
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC\_TOKIN/ 77.C3371.10L  
H/S: IRF8707 SO-8/14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037  
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37  
Switching freq-->350KHz

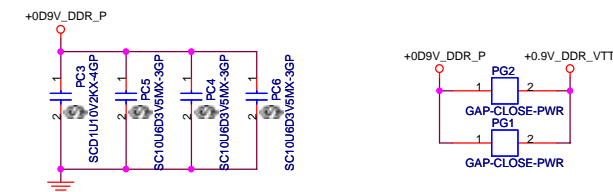
+1.05V\_SUSP/+/- 5%  
Design Current: 14.3A  
Peak current 20.4A  
22.44<OCP<28.5

$$V_{out} = 0.75V * (R1 + R2) / R2$$

<Core Design>

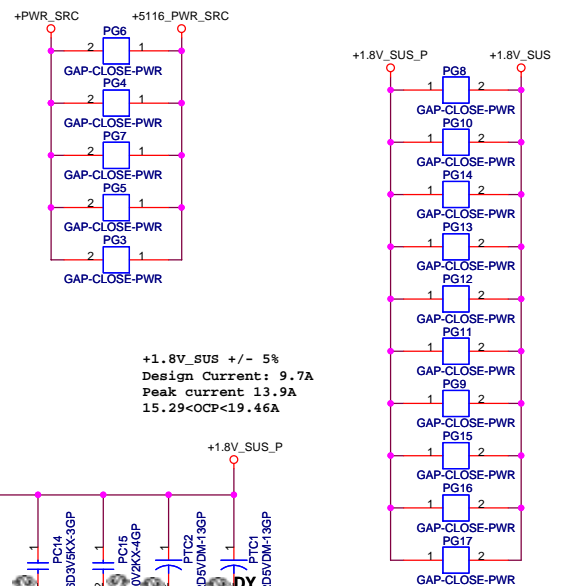
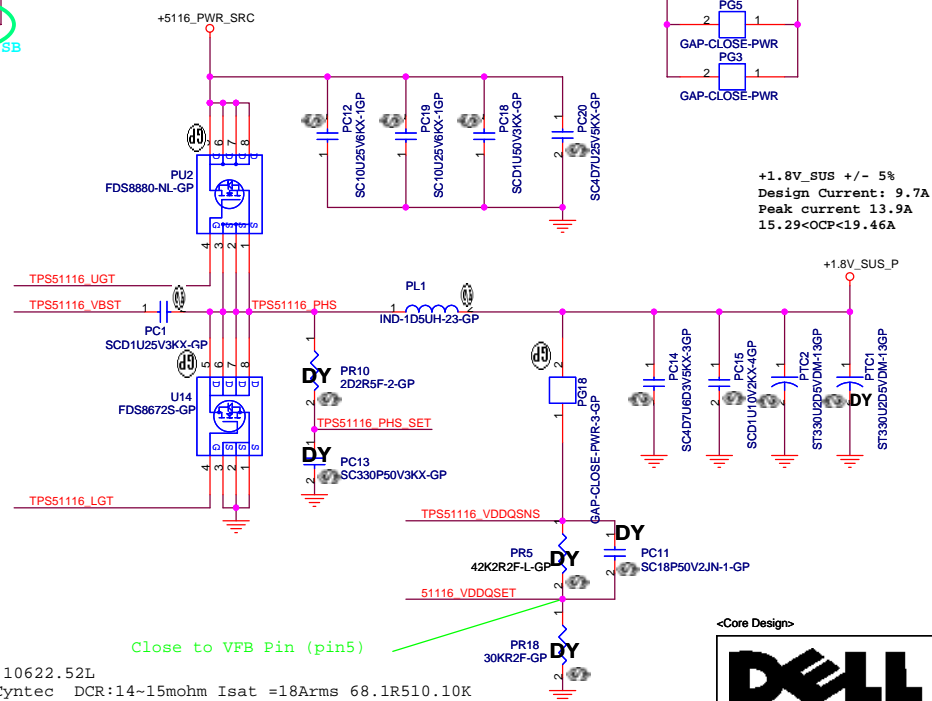
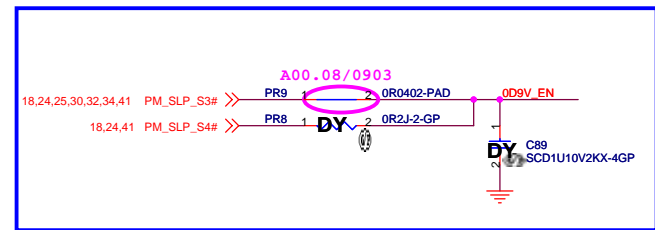
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
DC to DC 1.05V					
Size	Document Number				Rev
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## TI TPS51116 for 1.8V and 0.9V



VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

4/14 modify.  
Add RC circuit for power sequence.



+1.8V\_SUS +/- 5%  
Design Current: 9.7A  
Peak current 13.9A  
15.29<OCP<19.46A

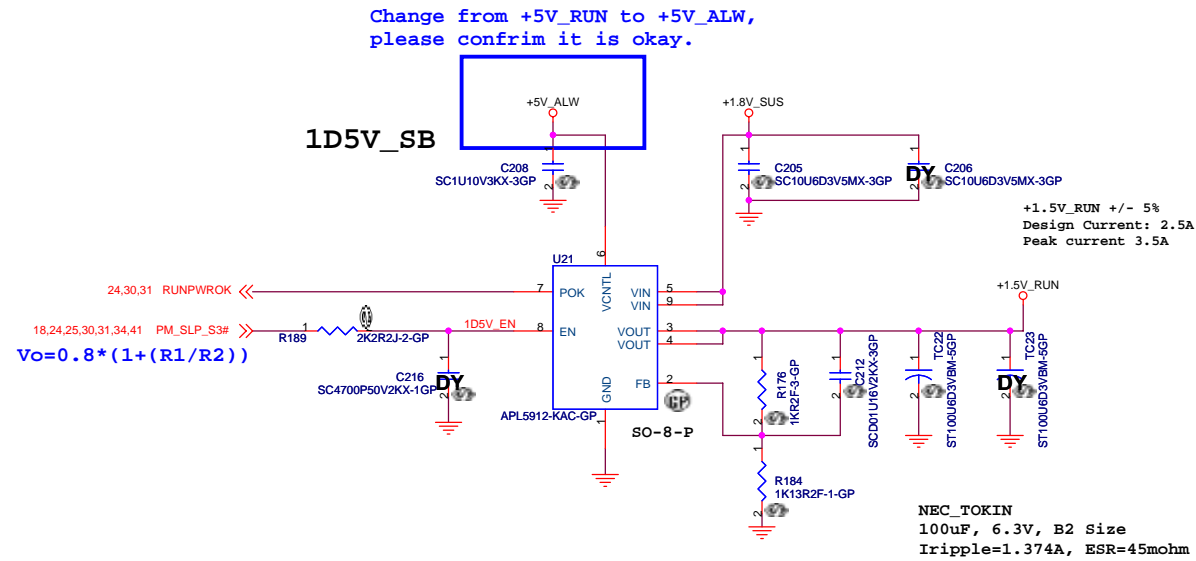
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Title			
<b>DC to DC 1.8V/0.9V</b>			
Size	Document Number		Rev
Custom	<b>DR2 17" UMA</b>		<b>2</b>
Date:	Monday, August 03, 2009	Sheet 31 of	59

SSID = PWR.Plane.Regulator\_1p5v




<Core Design>

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Title			
DC to DC 1.5V			
Size	Document Number	Rev	
Custom	DR2 17" UMA	-2	
Date:	Monday, August 03, 2009	Sheet	32 of 59



(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Custom

Document Number

Rev

**VGA Power**

**DR2 17" UMA**

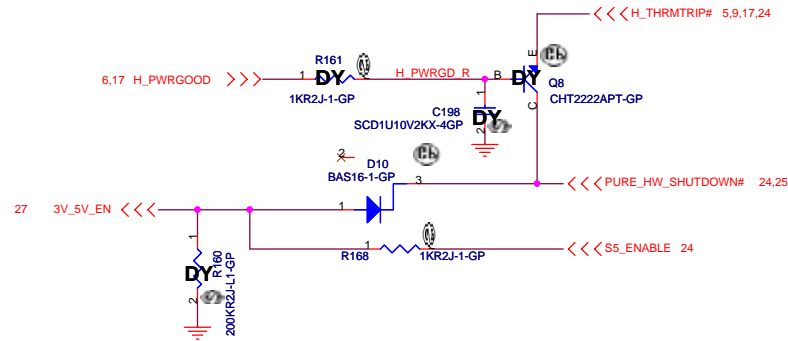
**2**

Date: Monday, May 18, 2009

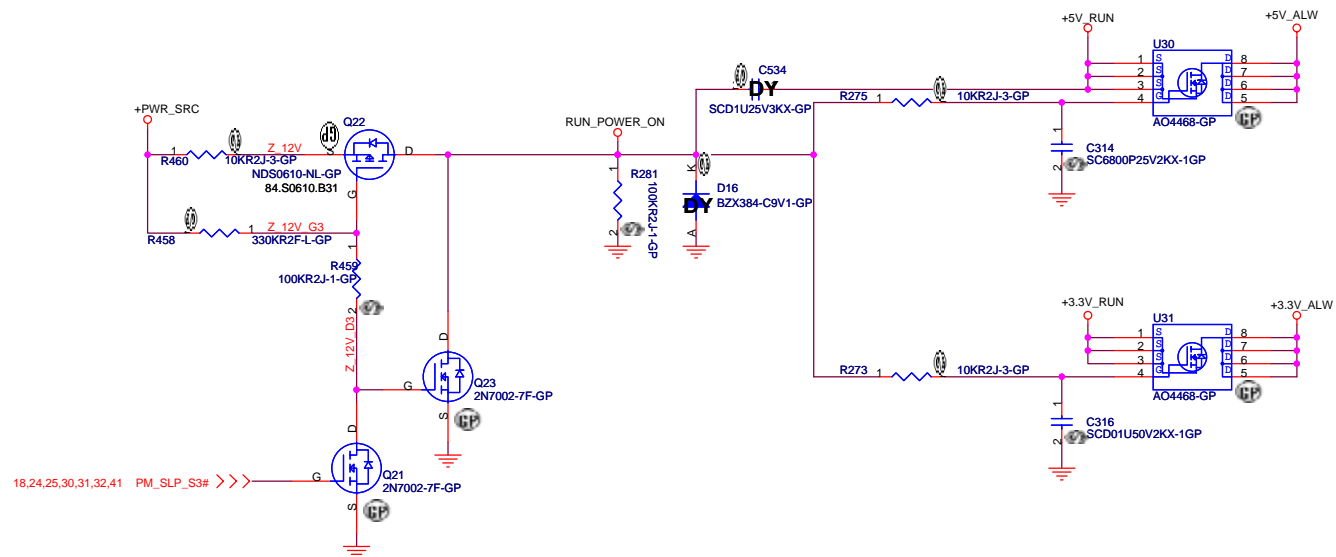
Sheet 33 of 59

1

SSID = Reset.Suspend



## Run Power



<Core Design>

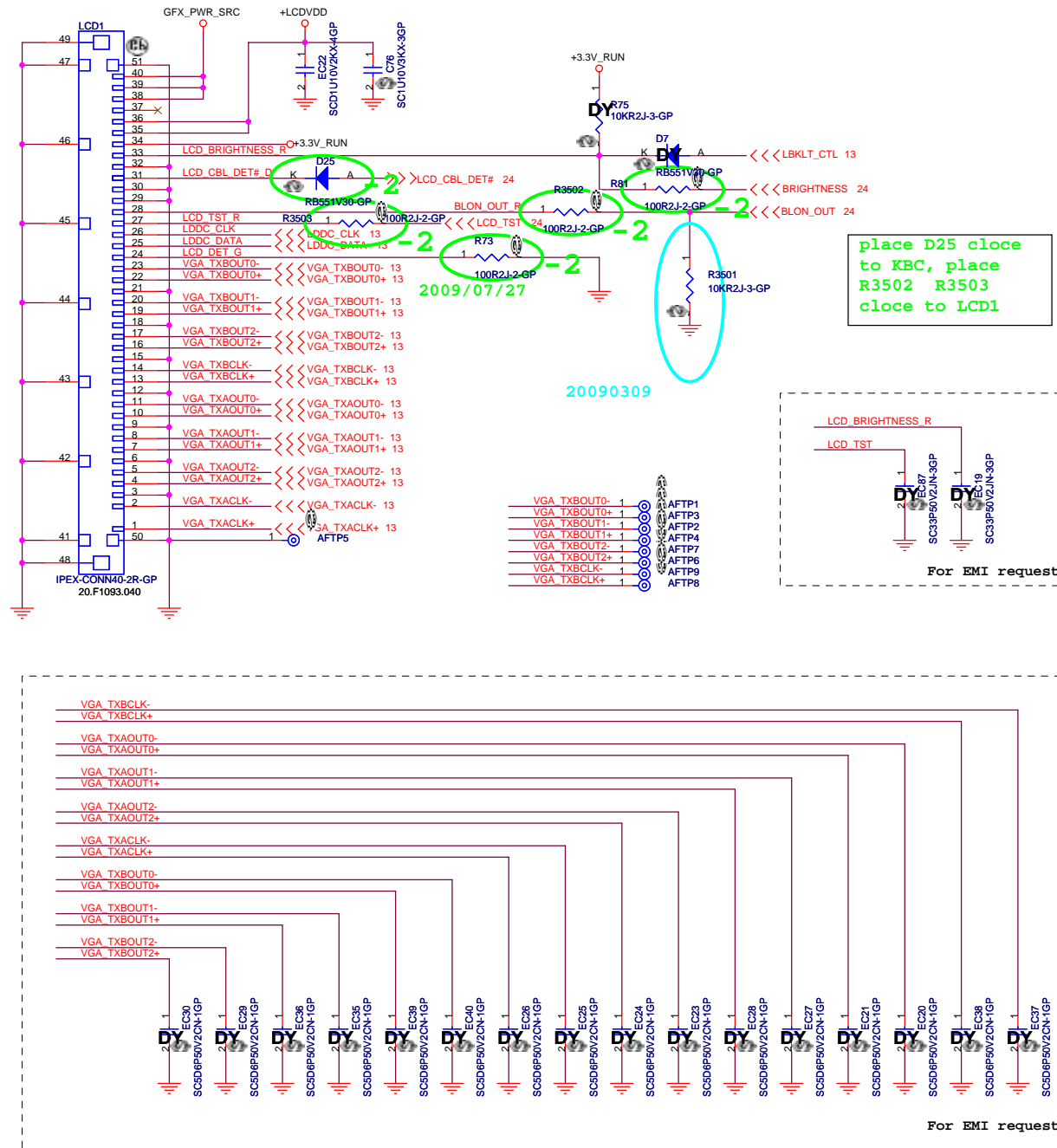


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Title			<b>Power Plane Enable</b>		
Size	Document Number		Rev		
Custom			<b>DR2 17" UMA</b>		<b>2</b>
Date:	Monday, August 03, 2009		Sheet	34	of 59

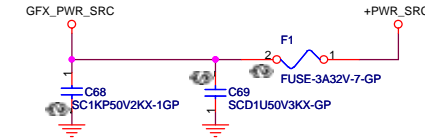
SSID = VIDEO

## LVDS CONNECTOR



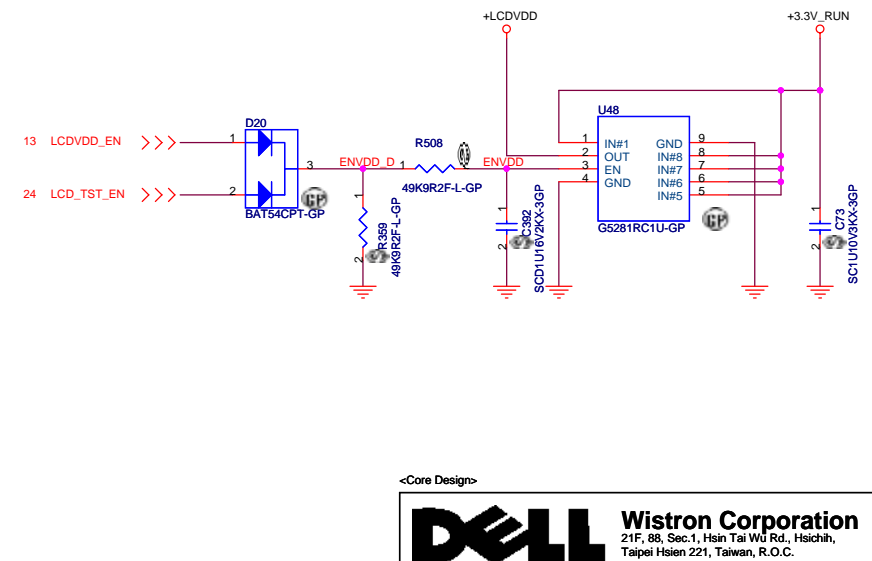
SSID = Inverter

## INVERTER POWER



SSID = VIDEO

## LCD POWER



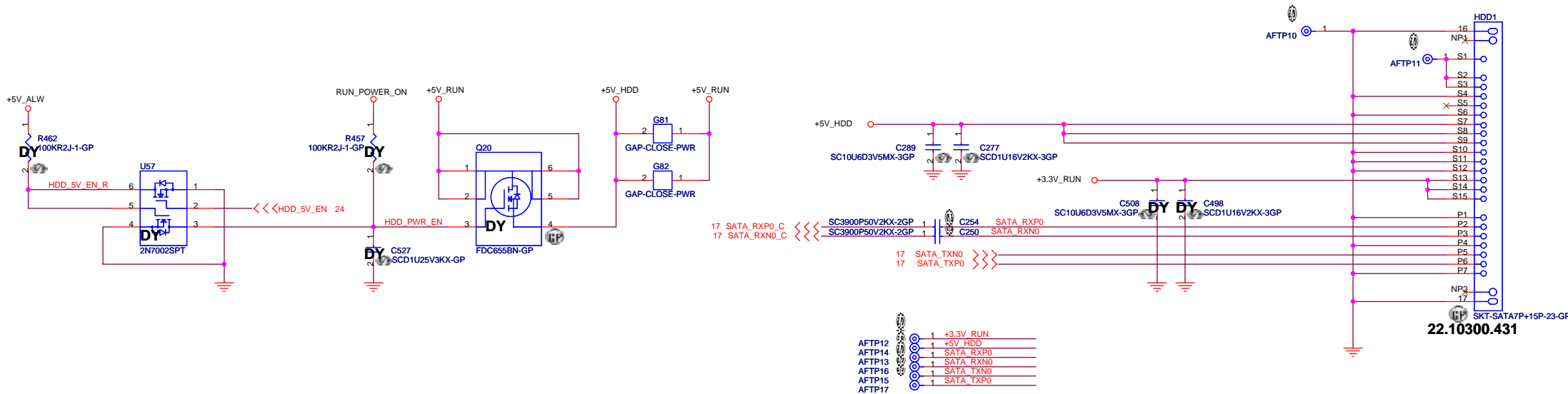
<Core Design>

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Title	LCD/Inverter Connector		
Size	Document Number	Rev	-2
Custom	DR2 17" UMA	Sheet	35 of 59
Date:	Monday, August 03, 2009	Sheet	35 of 59

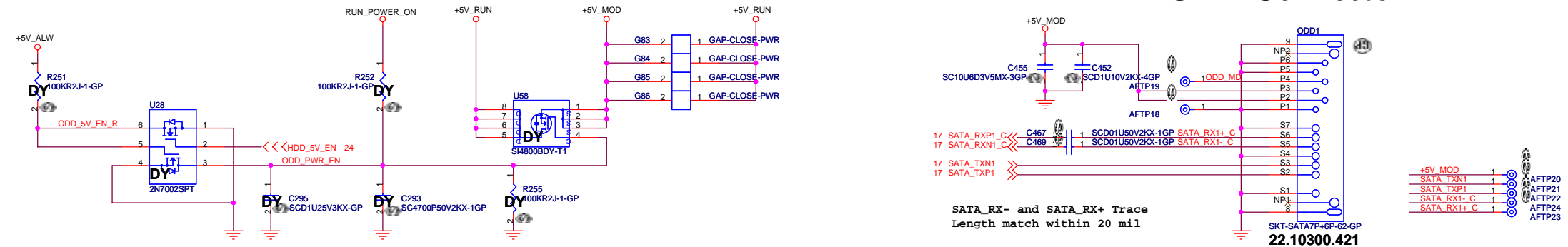
SSID = SATA

## SATA HDD Connector



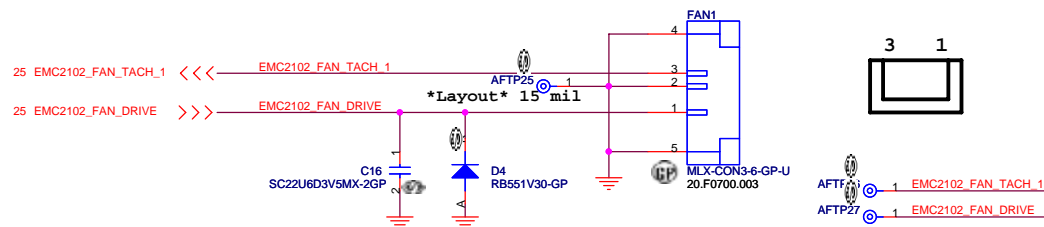
SSID = SATA

## ODD Connector



SSID = Thermal

## Fan Connector



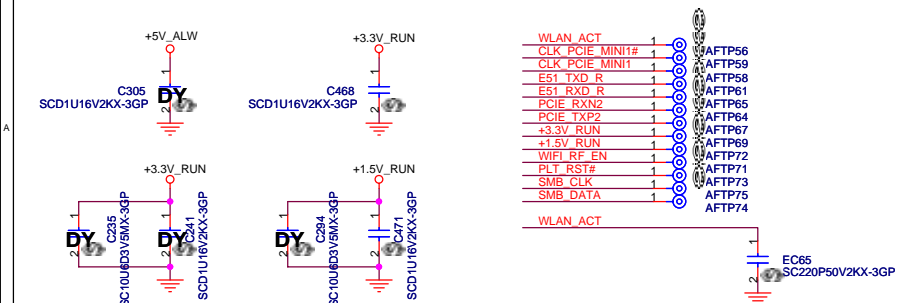
<Core Design>



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Title				<b>HDD/ODD/FAN</b>	
Size	Document Number			Rev	
Custom	<b>DR2 17" UMA</b>				<b>-2</b>
Date:	Monday, August 03, 2009		Sheet	36	of 59

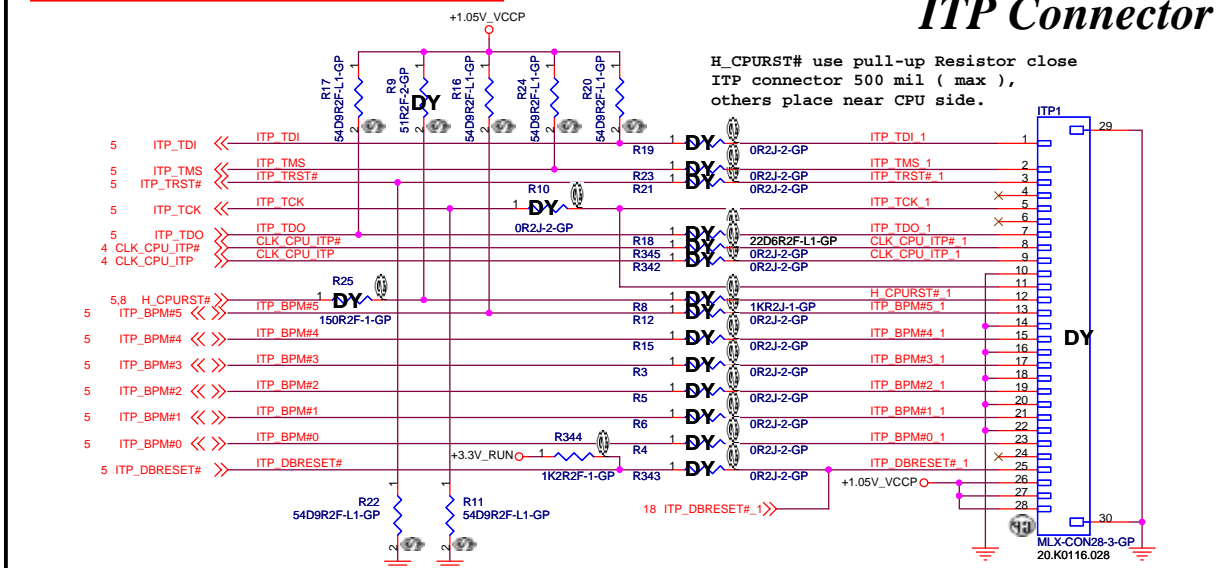
### Mini Card Connector(802.11a/b/g)



## *SD/XD/MS Card Reader*



## *ITP Connector*



```

graph LR
    subgraph CPU
        TCK_CPU[TCK(PIN AC5)]
    end
    subgraph ITP_Connector
        TCK_ITP[TCK(PIN 5)]
        FBO_ITP[FBO(PIN 11)]
    end
    TCK_CPU --- TCK_ITP
    TCK_CPU --- FBO_ITP

```

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

## <Core Design>




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Title		
<b>MINICARD(WLAN)/SD/TP CONN</b>		
Size	Document Number	Rev
Custom	<b>DR2 17" UMA</b>	<b>-2</b>
Date: Monday, August 03, 2009	Sheet 37	of 59

(Blanking)

<Core Design>



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Title


**MINICARD(WWAN)**

Size	Document Number	Rev
Custom	<b>DR2 17" UMA</b>	<b>2</b>

Date: Monday, May 18, 2009	Sheet 38 of 59
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(Blanking)

<Core Design>



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Title

**MINICARD(WPAN)**

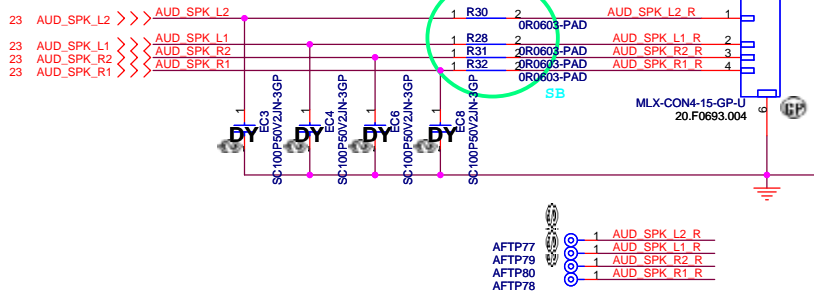
Size	Document Number	Rev
Custom	<b>DR2 17" UMA</b>	<b>2</b>

Date: Monday, May 18, 2009	Sheet 39 of 59
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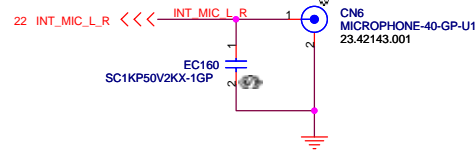


SSID = AUDIO

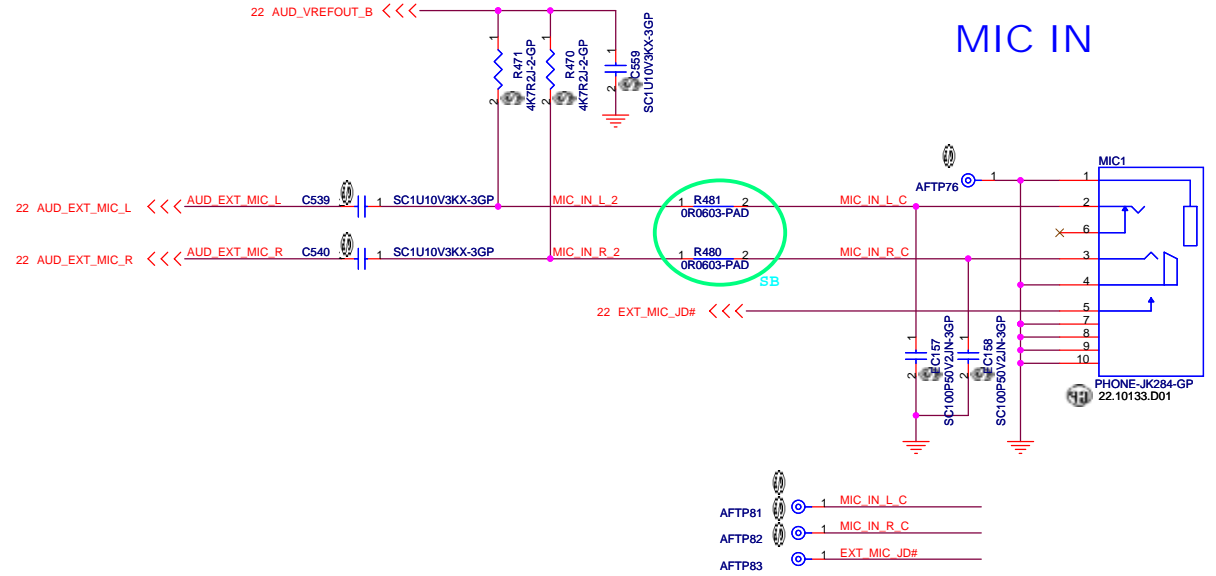
## Speaker Connector



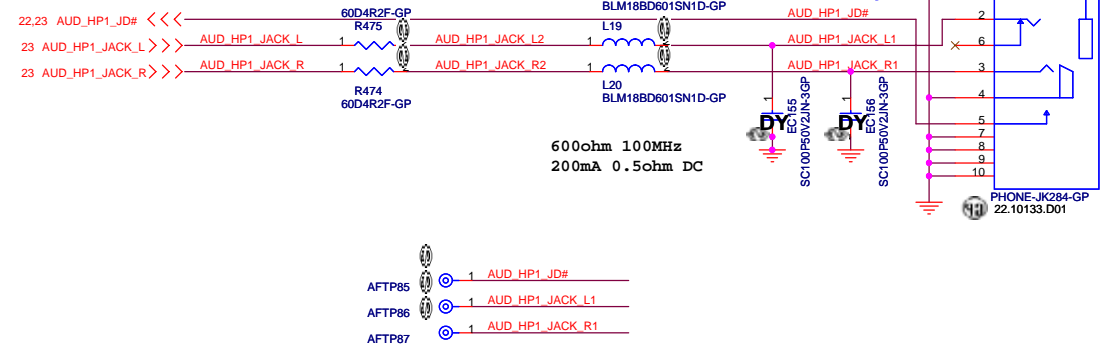
## Internal Microphone



## MIC IN



## LINE1 OUT

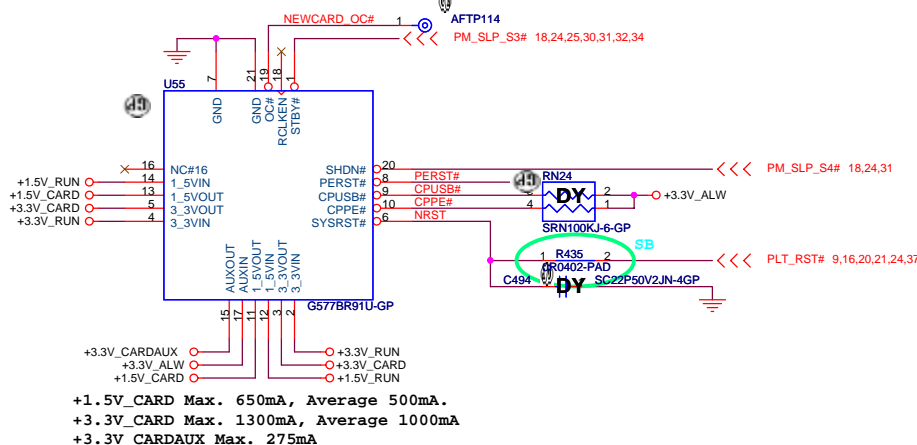
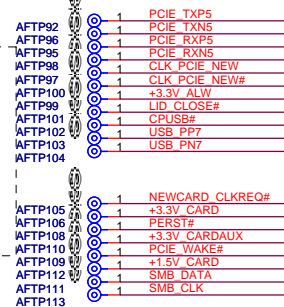
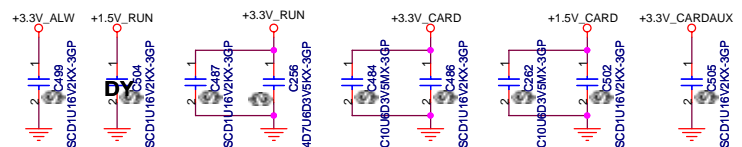


<Core Design>

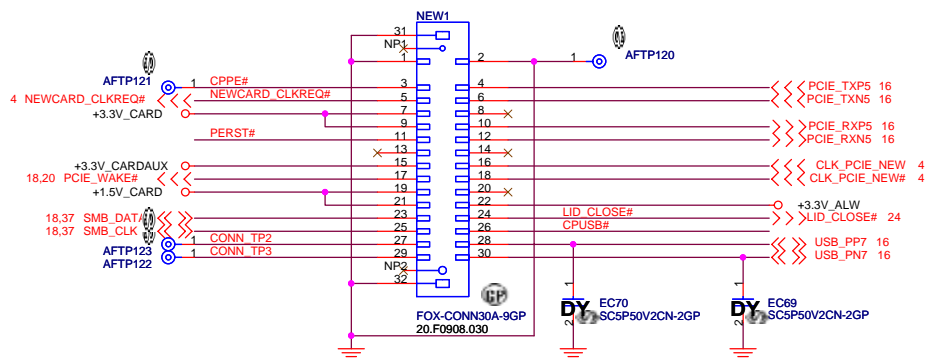
<b>DELL</b> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Audio Jack</b>		
Size Custom	Document Number <b>DR2 17" UMA</b>	Rev <b>2</b>
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```
SSID = ExpressCard
```

Place them Near to Chip

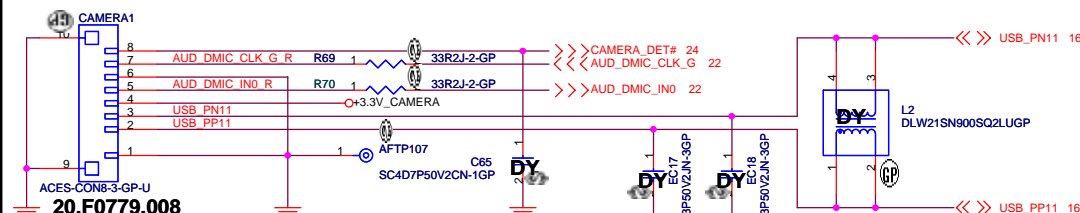


## New Card Connector

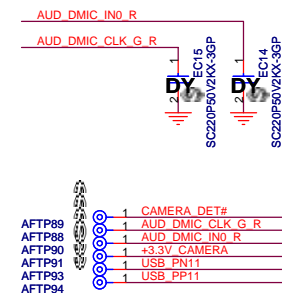
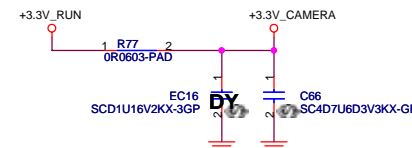


```
SSID = User.Interface
```

## Camera Connector

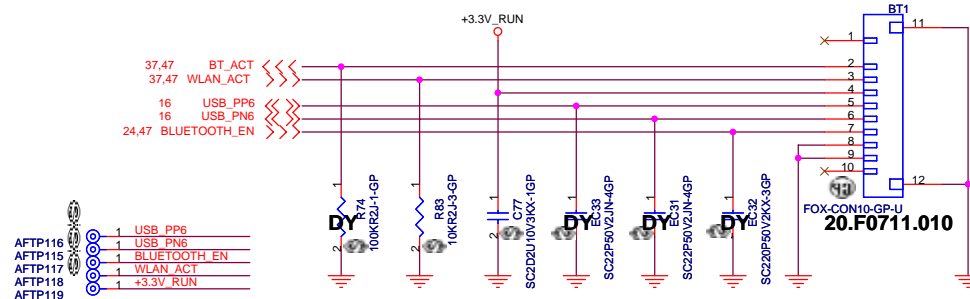


## Digital Mic Power



```
SSID = User.Interface
```

Bluetooth Module conn.



&lt;Core Design&gt;



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Title			
<b>Bluetooth/CAM/New Card</b>			
Size	Document Number		Rev
Custom		<b>DR2 17" UMA</b>	<b>-2</b>
Date:	Monday, August 03, 2009	Sheet 41 of	59

## SSID = Flash.ROM



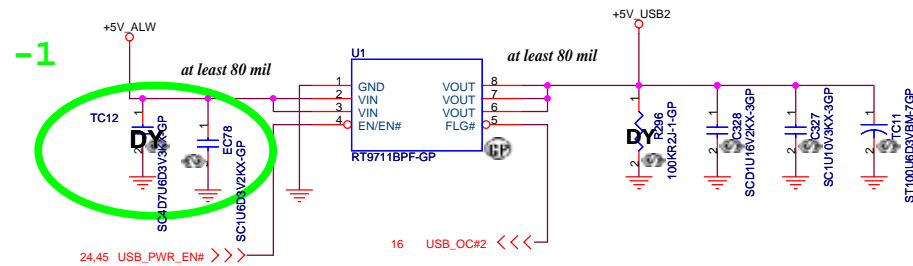
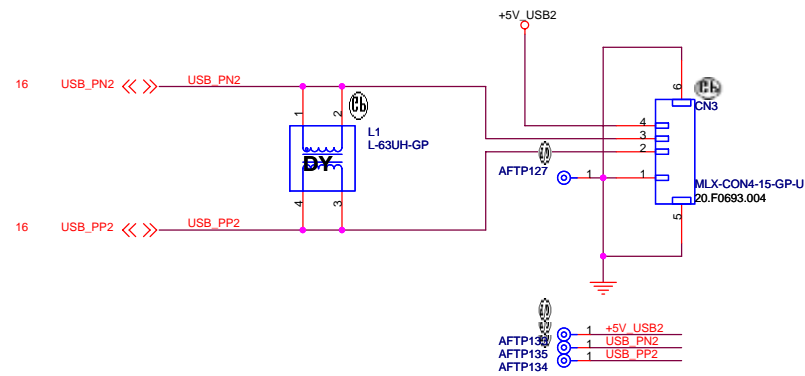
The diagram shows a power supply circuit. At the top left, there is a label "24 KBC\_PWRBTN# <<". Below it is a component labeled "DY" connected to ground. To its right is a transformer labeled "EC161 SC220P50V2KX-3GP". The secondary winding of the transformer is connected to a bridge rectifier consisting of four diodes. One diode is labeled "AFT124". The output of the rectifier is connected to a filter capacitor labeled "R500 100R2L-2-GP". A green circle highlights the capacitor R500 and the junction where the AC line enters. Above the capacitor, the date "2009/07/27" is written in green. To the right of the capacitor, there is a label "KBC\_PWRBTN# IN" next to a terminal. Further right, there are five terminals numbered 1 through 5, which are connected to a connector labeled "CN1". Terminal 6 is also shown but not connected. At the bottom right, there is a label "ACES-CN4#10-GP-U" next to a component symbol.

## SSID = RBATT

[illegible]

**SSID = USB**

## Right USB Port CONN



**<Core Design>**



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Title

## USB

Size	Document Number
Custom	

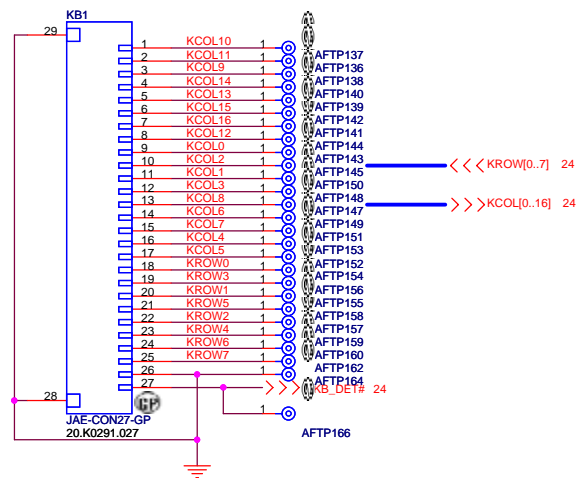
**DR2 17" UMA**Rev  
-2

Date: Monday, August 03, 2009

Sheet	43	of	59
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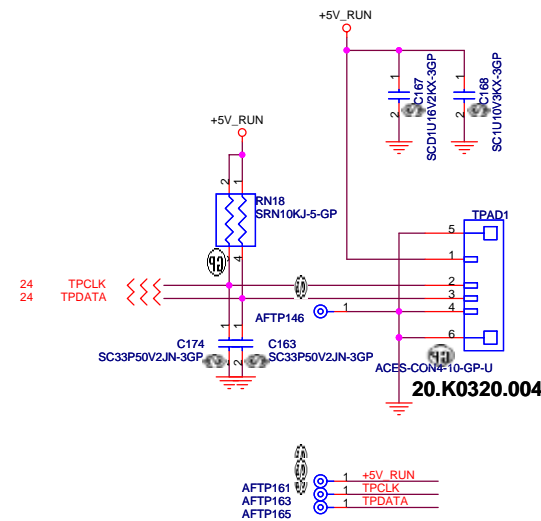
SSID = KBC

## Internal Keyboard Connector

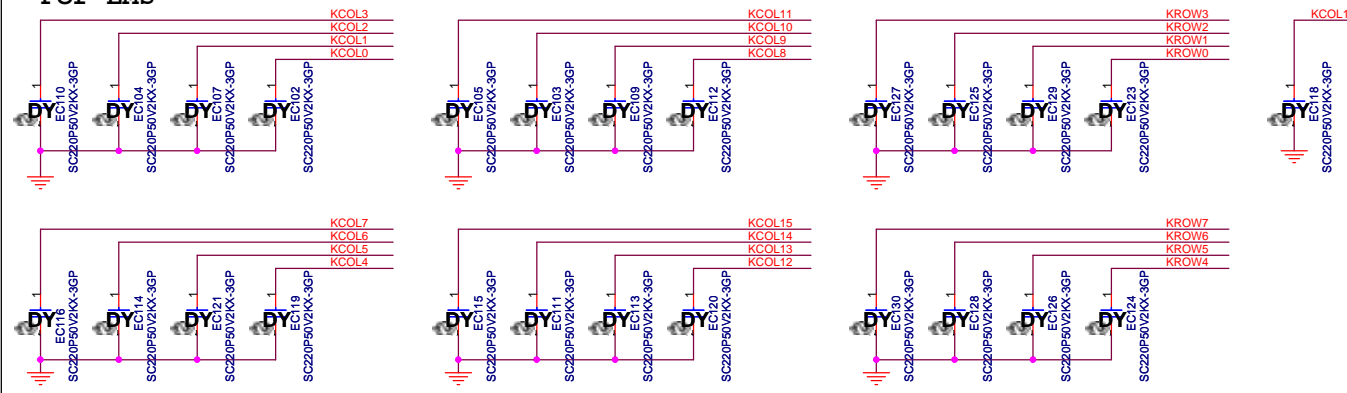


SSID = Touch.Pad

## TouchPad Connector



## For EMS

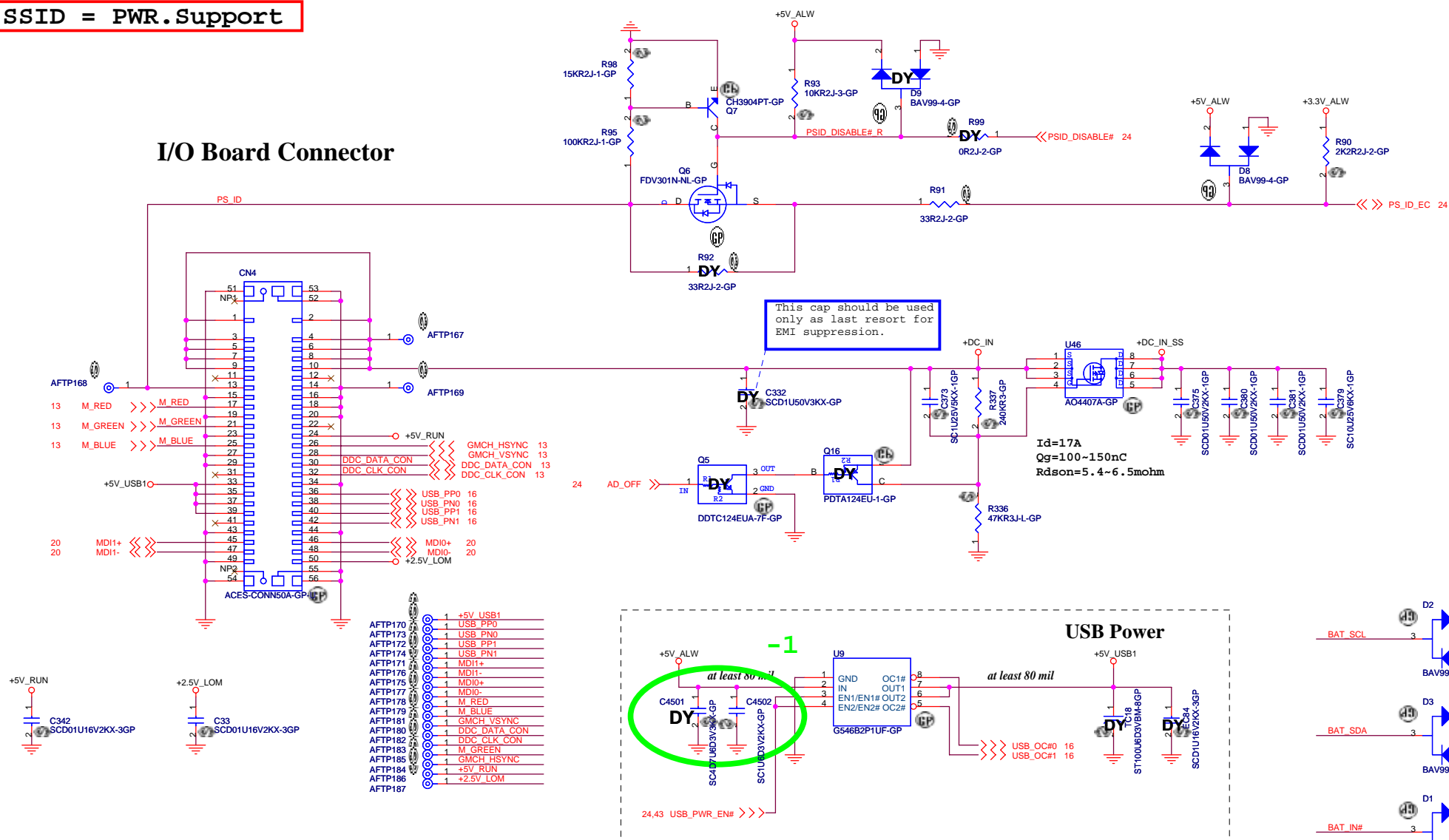


<Core Design>

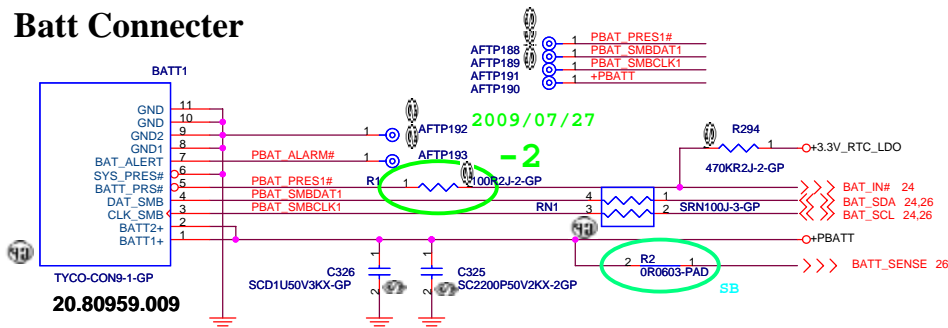
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>KeyBoard/Touch Pad</b>			
Size	Document Number	Rev	
Custom			
Date: Monday, August 03, 2009		Sheet 44 of 59	Rev -2

SSID = PWR.Support

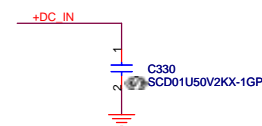
## I/O Board Connector



## Batt Connector



Reserved for EMI  
Place near DCIN1




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SSID = LOM

SSID = VIDEO

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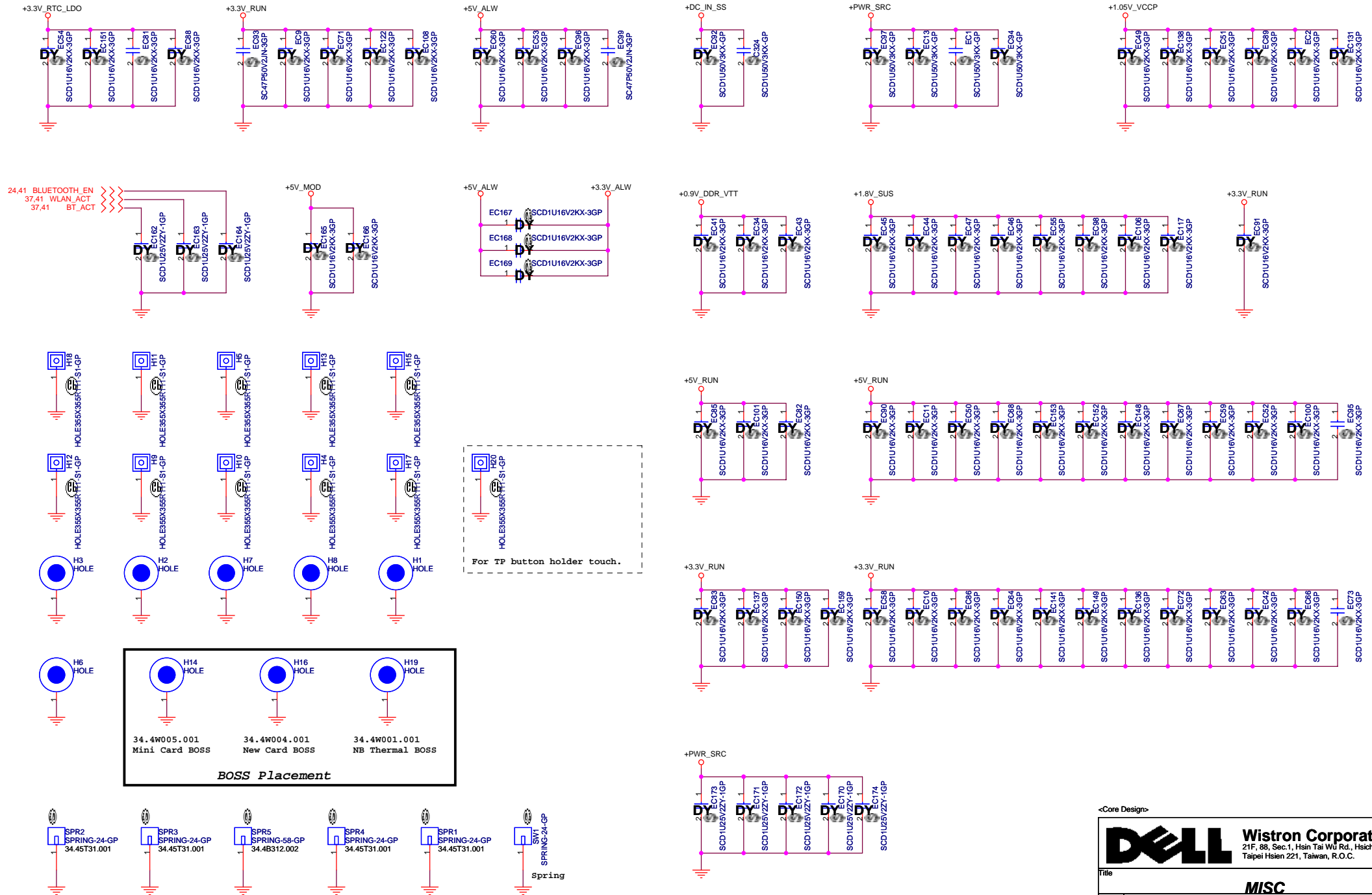
Title

***LAN CONNECTOR / CRT***

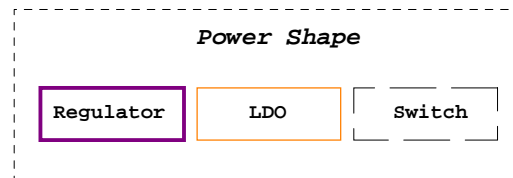
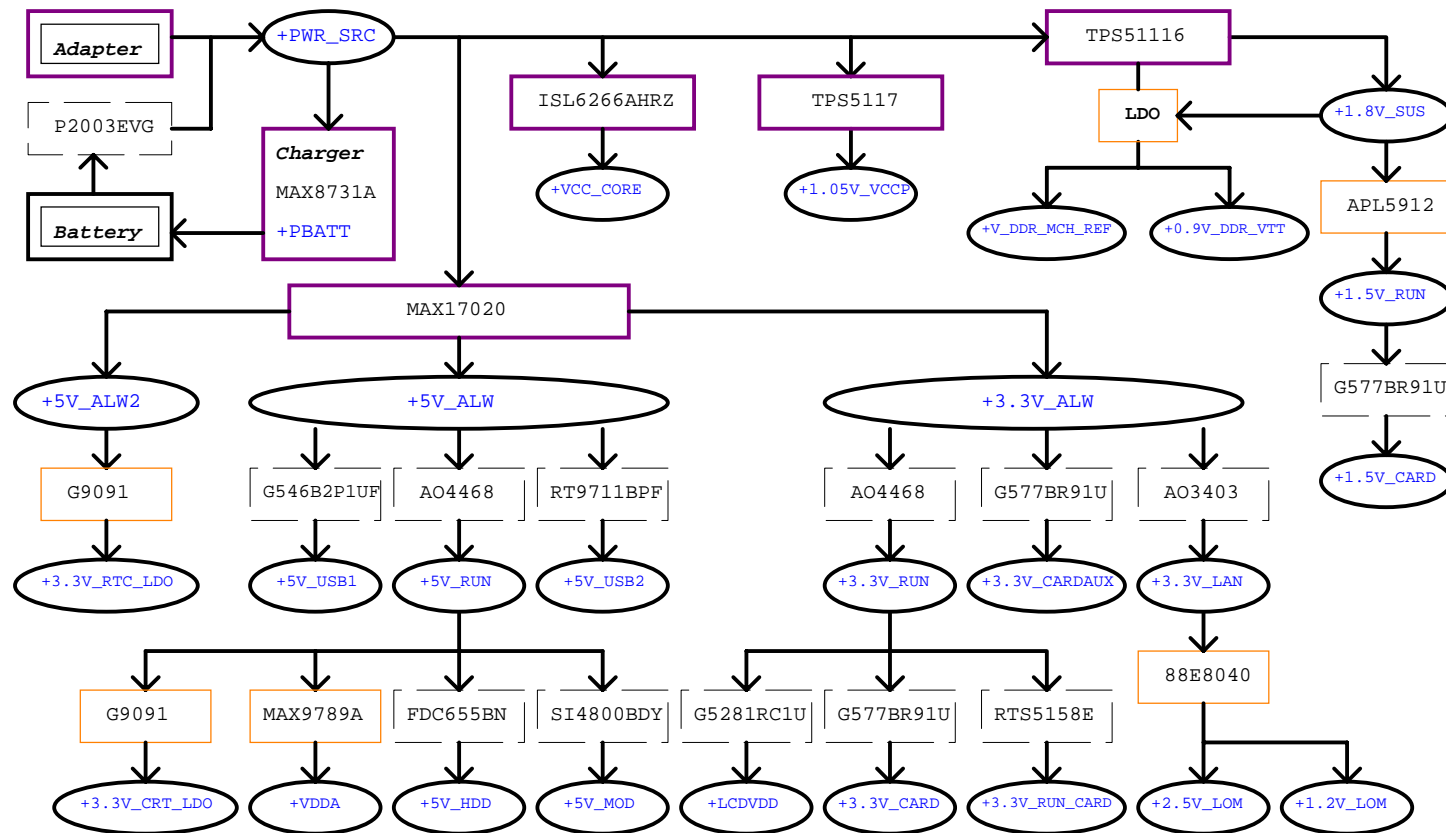
Size	Document Number	Rev
Custom	<b>DR2 17" UMA</b>	<b>2</b>

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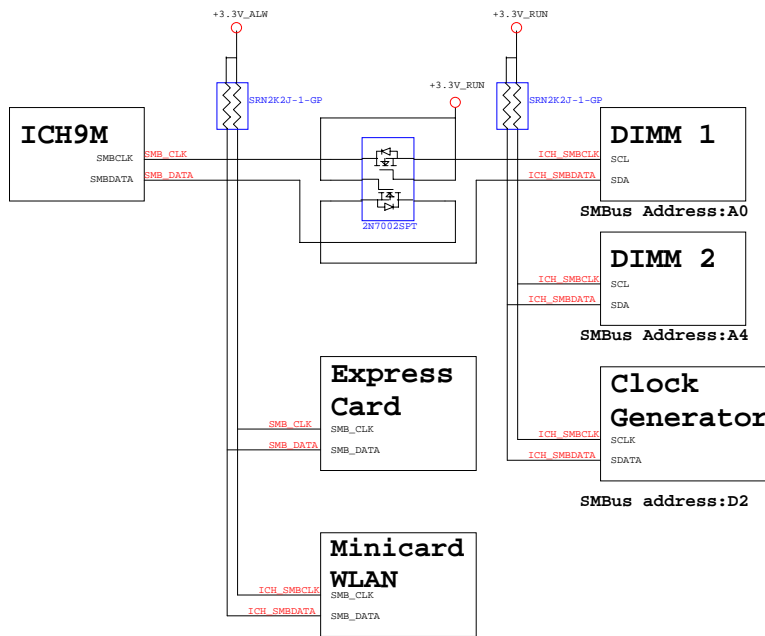




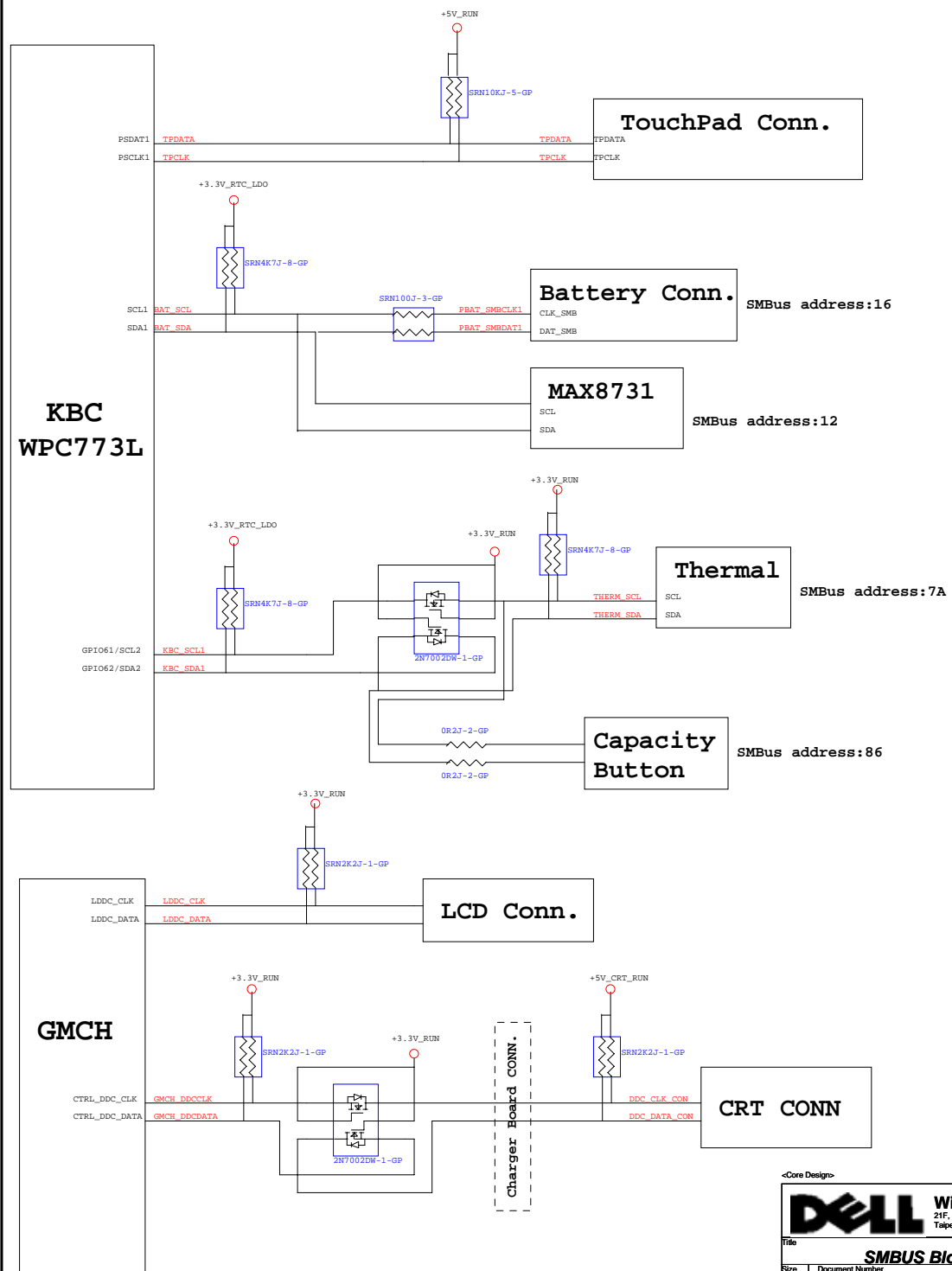
&lt;Core Design&gt;



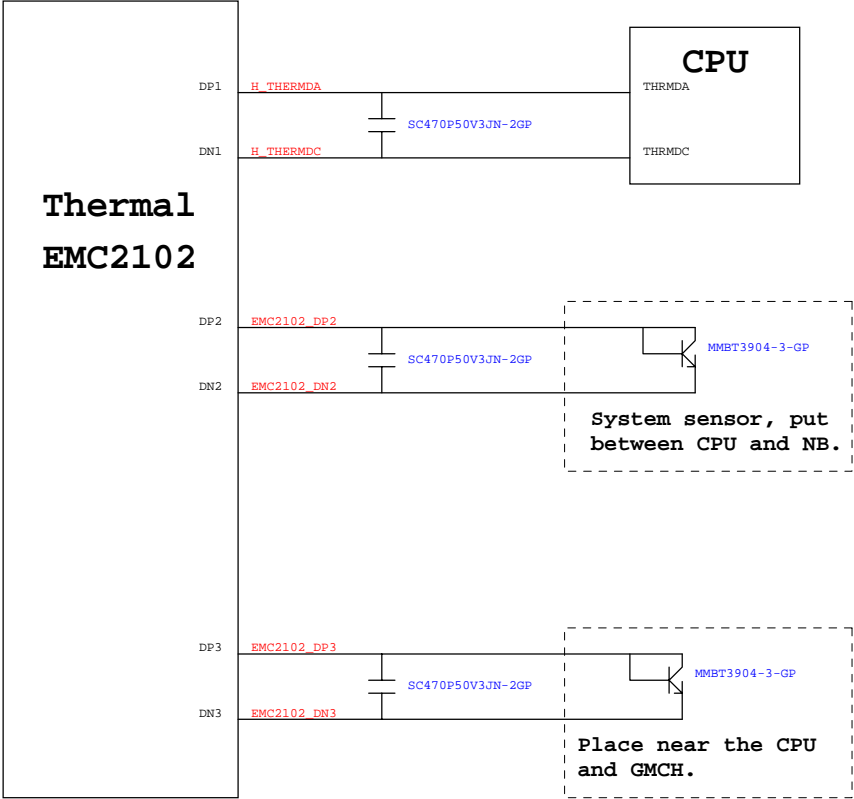
# ICH9M SMBus Block Diagram



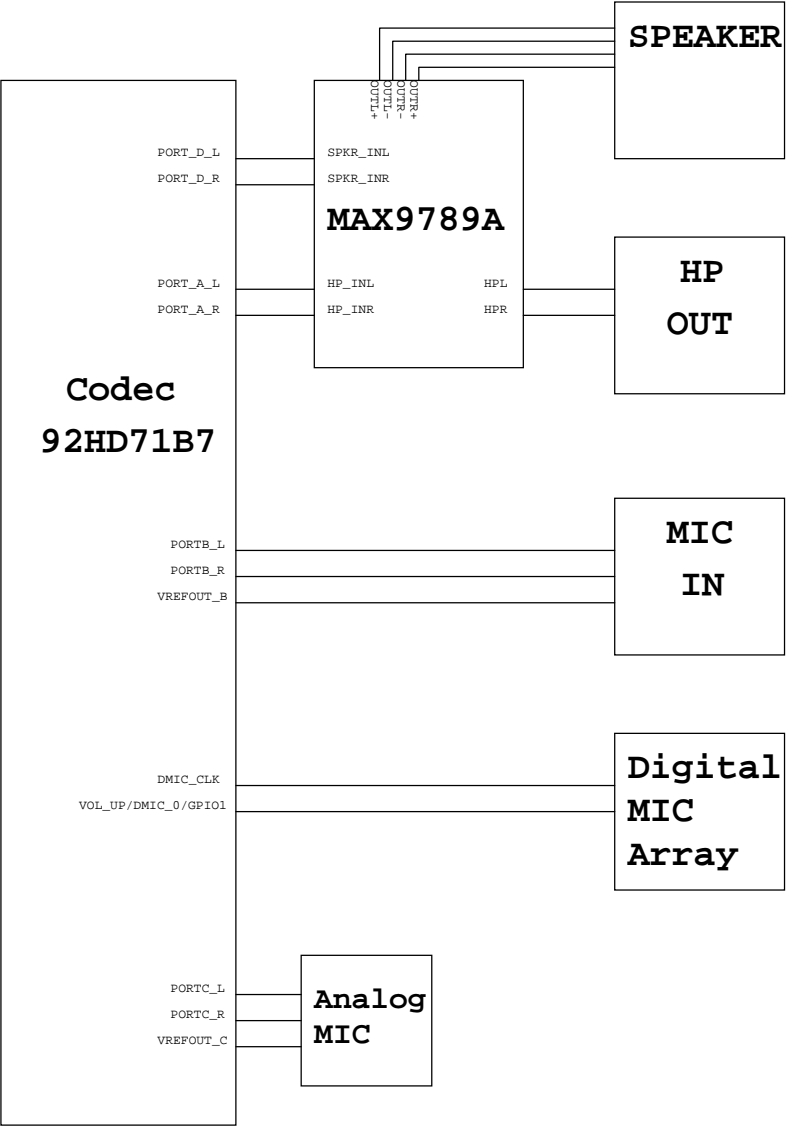
# KBC SMBus Block Diagram



# Thermal Block Diagram




# Audio Block Diagram



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Title

VGA-PCIE(1/4)

Size  
Custom


Document Number  
**DR2 17" UMA**

Rev  
**2**

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Title


VGA-VRAM(2/4)

Size	Document Number	Rev
Custom	DR2 17" UMA	2

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Title

**VGA-HDMI/STRAP(3/4)**

Size

Document Number

Rev

Custom

**DR2 17" UMA**

**2**


Date: Monday, May 18, 2009

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Title

VGA-LVDS/TV/CRT/(4/4)

Size

Custom

Document Number

DR2 17" UMA

Rev


2

Date: Monday, May 18, 2009

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( Blanking )

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

Custom

**DR2 17" UMA**

**2**

Date: Monday, May 18, 2009

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1

DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	45	CN4 Pin.51 from +DC_IN change to GND.	CN4 Pin.51 should be ground.	EE
		2	24	Dummy R422	LID SW is push-pull type, no need pull high.	EE
		3	41	CAMERA1 conn reduce from 10 to 8 pin.	Follow camera design.	EE
		4	42	RTC1 CONN change p/n: 22.70031.001 to 62.70001.011.	Qty issue to change another.	EE
		5	46	Exchange H14 and H6 names.	Correction. H14 for mini card boss ; H6 is hole.	EE
06/05		6	42	Reverse LED1.	Correction. Amber for BAT_LED_B ; White for PWR_LED_B.	EE
		7	37,41	Remove CN5 and related circuit in page.41. Add dummy R: R493, R494, R495, R496, R497, R498, R499	Remove debug board connector. For debug mini card, change LPC Bus to mini card base. Set dummy res to avoid damaging MB or additional mini card.	EE
		8	37	Dummy R210, R211	For debug mini card. Set dummy res to avoid damaging MB or additional mini card.	EE
		9	24	Dummy R150. Staff R151.	PCB Version for SB.	EE
06/06		10	42	CN1 Pin.2 set to NC. Add R500 and dummy EC161.	Avoid shorting between KBC_PWRBTN# and GND. New R and C are for EMC pre-location.	EE
		11	24	Dummy R406. Change R425, R422, R409, R406, R401, R404 to 100K ohm.	Dummy R406 for no keyboard detect function. R change to 100k for save power.	EE
06/10		12	36	Update HDD symbol.	Update symbol and footprint for only SATA HDD. (no co-layout)	EE
		13	35~45	Change All TP near connectors to AFTP (ZZ.AFT30.101).	For AFTE test pad.	EE
		14	04	Change C461 and C462 from 15pF to 12pF.	For X3 cap choice by report suggestion.	EE
06/12		15	17	Change C520 and C522 from 15pF to 12pF.	For X4 cap choice by report suggestion.	EE
		16	24,42	Add 0 ohm R482 on EC_SPI_WP# and link to KBC/GPIO30. Change RN50 to 100k and Add R476 for EC_SPI_WP#.	KBC can control WP# of Flash ROM. R change to 100k for save power.	EE
		17	40	Change L19 and L20 to 68.00082.531.	For EMI.	EE
		18	45	Change M_RED to CN4 Pin.17 ; M_GREEN to CN4 Pin.21 ; M_BLUE to CN4 Pin.25. CN4 Pin.23 and Pin.27 to GND.	Avoiding noise to impact CRT signals.	EE
		19	47	Add H20.	Add square GND for TP button holder touch.	EE
06/16		20	42	Dummy CN2, R34.	Cap. button function is disable.	EE
		21	47	Add dummy EC162, EC163, EC164. Add dummy EC165, EC166. Add dummy EC167, EC168, EC169.	For EMI.	EE
06/17		22	04	Change R216 to 22 ohm.	The same clock dirve to U25 and U34.	EE
06/18		23	44	Dummy EC110, EC104, EC107, EC102, EC105, EC103, EC109, EC112, EC127, EC125, EC129, EC123, EC118, EC116, EC114, EC121, EC119, EC115, EC111, EC113, EC120, EC130, EC128, EC126, EC124.	For EMI.	EE
06/19		24	43	Short R26, R27.	No need 0 ohm R.	EE
		25	47	Add SW1.	ME request.	EE
		26	35	LCD1.38 link to GFX_PWR_SRC ; LCD1.37 set NC ; LCD1.35 link to +LCDVDD ; LCD1.34 link to +3.3V_RUN ; LCD1.33 link to LCD_BRIGHTNESS ; LCD1.32 to GND ; LCD1.31 link to LCD_CBL_DET#.	For LED backlight panel.	EE
		27	18	Dummy R179, R423.	SW check vender ID by SMBus.	EE
		28	24	Dummy R416, R418.	Cap. button function is disable.	EE
		29	40	Change LOUT1 and MIC1 to 22.10133.D01.	Change jack source.	EE
		30	17,18	Dummy U25.B10 link R506 to GND; U25.C18 link R501 to GND; Dummy U25.C21 link R502 to GND; U25.C11 link R503 to GND; Dummy U25.AE18 link R504 to GND; U25.AF21 link R505 to GND. Dummy R421, R424.	Avoiding abnormal action in U25(ICH9-M).	EE
06/23		31	25	Change R82 to 20K 1% ; Change R78 to 10K 1%.	For T8 shutdown is set 88 deg-C.	EE
		32	47	Add dummy EC170, EC171, EC172, EC173, EC174.	For EMI.	EE
06/27		33	42	Change U23 to 72.25X16.A01.	Better performance.	EE

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<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Change List - EE (1/3)</b>			
Size A3	Document Number <b>DR2 17" UMA</b>	Rev <b>-2</b>	
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DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER	
07/30	X02	34	18	Staff R421, R424. (PT build cut-in)	Avoiding always issue interrupt event.	EE	
		35	23	Dummy R290 ; Staff R291. (PT build cut-in)	Adjust audio amp. gain value.	EE	
		36	20	Add dummy R507.	Add RUN power for LAN.	EE	
		37	21	Short R253, R254.	No need 0 ohm R.	EE	
		38	24	Staff R138, R150 ; Dummy R141, R151.	PCB Version for SC.	EE	
		39	35	Add R508 ; Change R359 to 49.9k ohm.	For LCD power sequence.	EE	
		40	22,23	Move C535 (Change 0.033uF), R472 to page.23. Remove C536 (Change 0.033uF), C542. Add R484 to gnd ; Add C566 for AUD_SET, C567 for AUD_BIAS. C565 for 6040 only.	For PC beep.	EE	
		41	36	Material change: HDD1	ME request.	EE	
		42	37	Material change: CARD1	ME request.	EE	
		43	47	Material change: SPR4	ME request.	EE	
		44	09	Add TP271 for U52/ SDVO_CTRLDATA.	TP.	EE	
		08/06	45	41	Short R79, R80.	No need 0 ohm R.	EE
			46	04	Symbol change: U54.	For clock generator co-layout.	EE
			47	-	Change to close line: R204, R200, R356, R139, R152, R408, R394, R390, R403, R402, R96, R120, R378, R360, R140, R373, R97, R405, R155, R154, R262, R266, R439, R265, R226, R269, R174, R175, R183, R432, R433, R434, R430, R431, R437, R191, R177, R270, R188, R436, R452, R259, R282, R250, R249, R467, R153, R81, R77.	No need 0 ohm R.	EE
48	24,32		Move R182 to page.24.	Movement.	EE		
49	37		Short R428, R426 ; Add DY L21.	Pre-location for Minicard USB trace.	EE		
08/07	50		-	Short R139, R96 , R155, R154, R226, R174, R175, R432, R433.	No need 0 ohm R.	EE	
08/11	51	19	Staff C488.	For DMI.	EE		
	52	23	Use 2.2uF C564 and C557 for Maxim U62 IC.	For improving bobo sound.	EE		
08/15	53	32	Material change: TC23. (DY)	Material issue.	EE		
09/02	A00	54	11	Material change: TC19, TC21.	Material issue.	EE	
		55	21	USB_PP10 for U34.5 ; USB_PN10 for U34.4. (ST build cut-in)	Schematic modification.	EE	
		56	24	Staff R151 ; Dummy R150.	PCB Version for -1(Xbuild).	EE	
		57	24	Add dummy R509 to gnd for KBC GPIO24. (09/10 update)	For GM45.	EE	
		58	05,17	Dummy R76 ; Staff R167	For H_THRMTRIP# to SB.	EE	
		59	12,20,24	Change to close line: R115, R246, R182, R158, R159, R170.	No need 0 ohm R.	EE	
		60	37	Remove L21.	No need L21.	EE	
		09/09	61	19	Staff R453, C511 ; DY C521.	Follow Intel DG 2.0.	EE
		09/10	62	04	Short RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN52, RN51.	No need 0 ohm R.	EE
		09/22	63	21	Add dummy R510 and C568. Staff R282 0 ohm.	For U34 power bounce issue.	EE
			64	04	Dummy R196.	For debug. Normally, no need it.	EE
			65	25	R82 change to 10k ; R78 change to 2.37k.	For T8 thermal shutdown setting.	EE
			66	23	Staff R288 ; Dummy R289.	For Audio amp. gain.	EE
		10/02	67	21	Dummy R284, C318. Staff R282 to Bead 68.00082.531. Staff R510 to 2.2K ; Staff C568.	For U34 power bounce issue.	EE

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05/18	-1	1	43	EC78 change to 1u	follow ul spec design	EE
		2	43	TC12 change to 4.7u	follow ul spec design	EE
		3	45	add c4501 and c4502	follow ul spec design	EE
		4	24	change R192 from short pad to 0ohm		EE
		5	42	change R419 from short pad to 0ohm		EE
		6	14/15	change R57 R54 R55 R56 from 0ohm to short pad		EE
DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER
07/27	-2	1	35	add D25	prevent GFX_PWR_SRC burn U20 by passing LCD_CBL_DET#	EE
		2	35	change R81 from short pad to 100ohm	For ESD	EE
		3	35	change R73 from 100R2F to 100R2J		EE
		4	35	add R3502 and R3503	For ESD	EE
		5	45/9	change R1 R94 from 100R2F to 100R2J		EE
		6	42	change R500 from short pad to 100ohm	For ESD	EE
		7	42	add R141,R146,R150. dummy R138,R143,R151	For MB VERSION ID	EE

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Title

Change List - EE (3/3)

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A3

Document Number  
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-2

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DATE	VERSION	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	32	R189 change to 2.2K ohm, C216 dummy.	For +1.5V_RUN sequence.	Power EE
		2	30	C378 change to 0.01uF.	For +1.05V_VCCP sequence.	Power EE
		3	34	C316 change from 4.7nF to 0.01uF.	For +3.3V_RUN sequence and improve +3.3V_ALW voltage drop due to SW(U31) turn on quickly (higher loading).	Power EE
		4	34	Staff C314 and change from 4.7nF to 6.8nF.	For +5V_RUN sequence and improve +5V_ALW voltage drop due to SW(U30) turn on quickly (higher loading).	Power EE
06/05		5	36	Dummy Q20, U57, R462, R457, C527 and U58, U28, R251, R252, C293, C295 Change R258, R256 to G81, G82 Change R278, R279, R277, R276 to G83, G84, G85, G86	No sniffer function, no control HDD & ODD power.	Power EE
06/06		6	27	R136 change to 270k and R108 change to 237k	For 5V/3.3V OCP	Power EE
		7	28	R38 change to 12.1k R323 change to 3.92k , C360 change to 0.047 uF 10V X7R	R38 for VCORE OCP R323 and C360 for transient and load line.	Power EE
		8	31	PC9 to GND.	PC9 to GND otherwise DC-DC IC can not obtain power to generate 1.8V/0.9V output.	Power EE
		9	31	PR2 change to 9.31k ohm.	For 1.8V OCP.	Power EE
		10	30	Add D23.	For power sequence.	Power EE
06/10		11	18,24	Remove U60, R482, R476 and change trace name VRMPWRGD to VGATE_PWRGD.	For power sequence.	Power EE
06/18		12	31	PR7.1 link to +5116_PWR_SRC.	Reserve for other source.	Power EE
06/23		13	30	Rename "+1.05V_SUSP" to "+1.05V_RUNP"	Correct naming.	Power EE
		14	26,45	Material change: U37, U46, U47.	NIKO-SEM P2003EVG component has some risk.	Power EE
07/30	X02	15	31	Change PR7 value from 622k to 619k ohm.	For 2nd source.	Power EE
08/11		16	26,45	Material change: U37, U46, U47.	Power team request.	Power EE
09/03	A00	17	26,27, 28,31	Change to close line: R46 ,R137 ,R127,R106 ,R384 ,R391 ,R35 ,R29 ,R307 ,R308 ,R309 ,R303 ,R304 , R298 ,R301 ,R310 ,R313 ,PR14.	No need 0 ohm R.	Power EE
		18	26	R61 change 4.7k to 10k.	Power team request.	Power EE
XX		19 20 21 22				
XX						
XX		23	x	x	x	Power EE
XX		24	x	x	x	Power EE
	25	x	x	x	Power EE	